Why is CMOS scaling coming to an END?

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***Abstract*—The continued physical feature size scaling of complementary Metal Oxide Semiconductor (CMOS) transistors is experiencing asperities due to several factors, and it is expected to reach its boundary at size of 22 nm technology by 2018. This paper discusses and analyzes the main challenges and limitations of CMOS scaling, not only from physical and technological point of view, but also from material (e.g., high-k vs. low-k) and economical point of view as well. The paper also addresses alternative non-CMOS devices (i.e., nanodevices) that are potentially able to solve the CMOS problems and limitations.**

Key words: *CMOS, constant-field scaling, lithography, dynamic/static power, high/low-k materials, nanodevices.*

I. Introduction

The concept of 'More Moore" refers to the continued scaling of horizontal and vertical physical feature sizes of silicon-based *complementary metal oxide semiconductor (CMOS)* transistors [1]. This tremendous effort has been the main impetus in producing today's sophisticated technologies of electronics devices. The scaling theory that proposed by Dennard et al. in 1972 is the starting point of this success story [2]. However, semiconductor industry starts to practice this theory in CMOS transistors a decade later. Since then, more and more transistors were able to be integrated into single integrated circuit (IC) chip. In 1965, Gordon E. Moore predicted that the number of transistors which can be placed in cutting-edge IC chips is doubling approximately every two years without correspondingly increasing the cost of the chips [3].

Although the scaling of CMOS transistors has past through some 'brick wall" predictions as reported in [4], pessimists believe that it will finally reach the boundary at size of 22 nm as forecasted in the International Technology and Roadmap for Semiconductors ITRS 2007 [1], approximately at the end of next decade. They frequently cite that CMOS transistors are approaching atomistic and quantum mechanical physics boundaries [5]. Furthermore, the concern is not only about the inability of the devices itself to continue operate steadily but also the constraints from the economic and technology point of view.

This paper addresses the important challenges that could hinder CMOS from being utilized in future. It divides the challenges into five categories, specifically:

- **Physical challenges**: These are due to the increment of tunneling and leakage currents as the devices are becoming smaller, thus impacts the performance and functionality of CMOS devices.
- **Material challenges**: These basically come from the inability of the dielectric and wiring materials to provide reliable insulation and conduction, respectively with continued scaling.
- **Power-thermal challenges**: These are because of the ever increasing number of transistors integrated per unit-area, which demands larger power consumption and higher thermal dissipation.
- **Technological challenges**: These are the results from the incompetency of lithography-based techniques to provide the resolution below the wavelength of the light to manufacture to CMOS devices.
- **Economical challenges**: These are mainly due to the rising in cost of production, fab, and testing that may reach a point where it will be not affordable from economic point of view.

In this paper, each of the above challenges will be analyzed. Alternative *non-CMOS nanodevices* that are possible to solve the CMOS limitation will be also presented.

The remainder of this paper is organized as follows. Section II give a brief overview about the principle structure and electrical parameter of *metal oxide semiconductor field-effect transistors (MOSFETs)* in order to facilitate the readability of the rest of the paper. Section III, IV, V, VI, and VII discuss in detail the physical, material, power-thermal, technological, and economical challenges of CMOS technology, respectively. Section VIII suggests potential non-CMOS nanodevices that are able to solve CMOS limitations. Finally, Section IX concludes the paper.

II. MOSFET Device Overview

Before we go further, we first overview the principle structure and important parameters of the core unit of CMOS i.e. MOSFETs. It will give us firm understanding of the scaling problems. The name 'metal-oxide-semiconductor' represents the materials used to form the early fabricated MOSFETs. Figure 1 shows the typical structure of a MOSFET with the three material layers: the metal gate electrode, the gate dielectric, and the silicon substrate. Nowadays, the metal gate electrode and silicon oxide-based gate dielectric have been replaced by polycrystalline silicon and high-k material such as Hf-based Zr-based, respectively [6].

The source and drain are formed by adding impurity dopant into substrate. The semiconductor material in the source and

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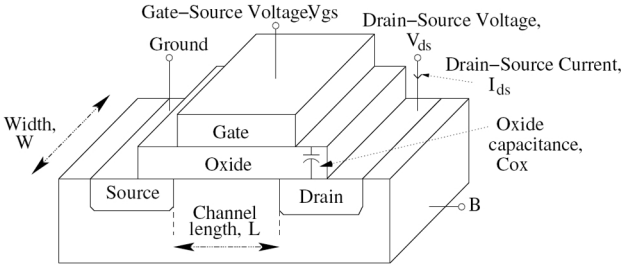

Fig. 1. Important MOSFET parameters.

drain region is doped with a different type of material than in the region under the gate. For example, if the substrate is doped with positive type (p-type) material such as Boron, the source and drain will be doped by negative-type (n-type) material such as Arsenic. In this case, an n-channel MOSFET (n-MOSFET) will be realized.

The area between source and drain beneath the gate, channel, has length of L and width of W; it is where the inversion layer is formed when sufficient voltage is biased to the gate and drain which then turn on the MOSFETs. The oxide layer with certain thickness, t_{ox}, separate the gate and the channel. According to [9], L and t_{ox} of 35 nm and 1.2 nm, respectively, have been demonstrated in 65 nm technology node.

There are few important parameters that determine the characteristics of MOSFETs (see Figure 1):

- Oxide capacitance, C_{ox}, is the capacitance per unit area between the gate metal and the bulk surface.
- Gate-source voltage, V_{GS}, is the voltage that applied between gate and source to control the operation of the transistor.
- Drain-source voltage, V_{DS}, is the voltage which is applied between drain and source.
- Threshold voltage, V_T, is the minimum voltage that will induce inversion layer which turn on the transistor.
- Drain-source current, I_{DS}, is the current that flow between drain and source through the inversion channel conducted beneath the gate when transistor is turned on.

III. Physical Limitation

The basic idea of constant-field scaling of CMOS transistors' physical feature and their corresponding band diagram are shown in Figure 2. For the original device as depicted in Figure 2(a), the channel have length of L, oxide thickness of t_{ox}, bias voltage of V and substrate doping of N_a. While the scaled device in Figure 2(b), all parameters are affected by the scaling factor, $s \approx 0.7$ [11]. The channel length is reduced to be $L \times s$, oxide thickness becomes $t_{ox} \times s$, bias voltage is decreased to be $V \times s$, and substrate doping is increased to be N_a/s.

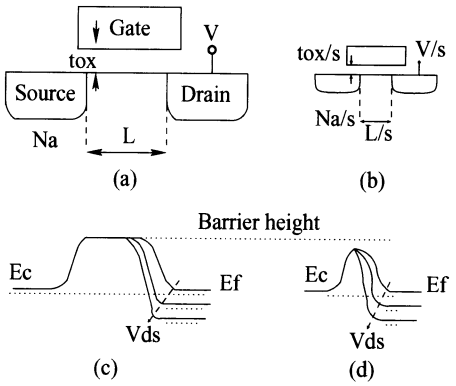

Fig. 2. CMOS constant-field scaling idea.

A. Decreasing devices dimension

The scaling of physical dimension includes the reduction in gate dielectric thickness and channel length; they are addressed next.

1) Gate dielectric thickness: The gate electrode together with gate dielectric control the switching operation of CMOS transistors. The voltage of the gate electrode controls the flow of electric current across the transistor. The gate dielectric should be made as thin as possible to increase the performance of the transistor. In additional, it is critical to keep short-channel effects under control when a transistor is turned on and reduce subthreshold leakage when a transistor is off. In order to maintain the electric field as CMOS transistors are scaled, the gate dielectric thickness should also be shrunk proportionally. An oxide thickness of 3 nm is needed for CMOS transistors with channel lengths of 100 nm or less [7]. This thickness comprises only a few layers of atoms and is approaching fundamental limits which is around 1 to 1.5 nm [8]. The thin oxide layer is subject to quantum-mechanical tunneling, giving rise to a gate leakage current that increases exponentially as the oxide thickness is scaled down. This tunneling current can initiate a damage leading to the fallible of the dielectric [9].

2) Short channel: Short channel enables faster switching operation since less time is needed for current to flow from source to drain. Howbeit, several negative effects could arise from it. A high off-state drain leakage current, I_{off}, flow even though the transistor is turned off. The band diagrams in Figure 2(c) and (d) represent the energy barrier that majority carriers in the source terminal needs to overcome to enter the channel for the original device and scaled version, respectively. As we can see in Figure 2(d), the barrier height is lowered thus reduces the threshold voltage used to form a depletion layer. Both ends of this short-channel may merge when a sufficiently large reverse-bias voltage is applied to the drain terminal. Consequently, many majority carriers start to flow from source to drain even if the gate voltage is below the threshold value, which result in punch-through, drain-induced barrier lowering (DIBL) [11] and threshold voltage roll-off [12]. These three problems cause drop in threshold voltage level, subsequently leakage currents [12].

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B. Lowering power and threshold voltages

Scaling the power supply voltage enables the reduction in dynamic power dissipation. While reducing the power supply of a chip might seem straightforward, nevertheless, it leads to issues such as noises and possibly signal levels compatibility problems in multichip systems using various supply voltages [10]. Reduction in power supply, which also reduces threshold voltage also increases static power during transistor off due to leakage current. In [12], an analysis of the impact of supply voltage scaling on the noise margin of CMOS NAND was performed; it concludes that the supply voltage cannot be scaled lower than 0.5 V in order to keep logic state consistency in the worst-case switching scenario. As threshold voltage is reduced as well, the transistor cannot be completely turned off. The transistor operates in a weak-inversion mode, with a subthreshold leakage between source and drain. The reduction of threshold voltage of about 85 mV will increase the subthreshold leakage current by 10 times [11]. Hence, it results in degradation of power and speed efficiency.

C. Increasing channel doping

In order to control short channel effects, it is desirable to increase the channel doping. However, this effort introduces other effects such as slower carrier mobility and band to band tunneling [13]. In a heavily doped channel, carrier mobility decreases severely due to high transverse electric field and impurity scattering. The on-state drain current, I_{on}, is reduced due to larger capacitance in high depletion-charge channel. In addition, a high channel doping will also result in band to band tunneling leakage. Furthermore, the formation of shallow channel due to thermal budget of dopant activation causes higher resistance thus reduces drain current [11]. Greater dopant concentration also causes gate-induced drain leakage current (GIDL) [14]. Therefore, increasing the channel doping will negatively impact the CMOS performance and functionality.

In summary, scaling efforts were successful in incrementing CMOS performance, reducing power consumption, while keeping high quality and reliable devices. Today, nonetheless, these efforts are becoming hard to realize, as the technology node approaching to limit (e.g. 10 nm).

IV. Material Limitation

New materials are introduced in order to keep up with the scaling of CMOS transistors. Figure 3 shows the changes in three decades starting in 1980 [15], [16]. This effort is done in order to ensure the manufacturability and reliability of devices.

Material such as Silicon (Si), Silicon dioxide ($Si0_2$), Aluminum (Al), Copper (Cu) and Salicides are bounded by their physic capabilities such as relative dielectric constant (ϵ), carrier mobility (μ), carrier saturation velocity (v_s), breakdown field strength (E_c) and conductivity [17]. As these material reach their physical limit, devices cannot keep up

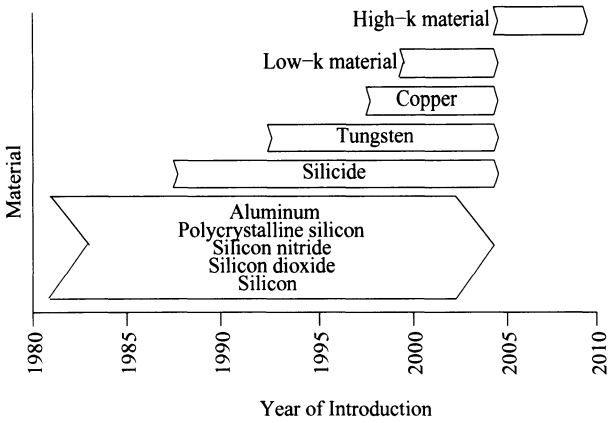

Fig. 3. Introduction of new materials.

with their performance. The SiO_2 reliability degrades as it becomes thinner and result in breakdown [4]. Although Cu is less sensitive to electromigration than Al, the material is more susceptible to open defect when used as interconnect wires. Low-k materials utilized for back end process (e.g. insulator between adjacent interconnect wires to minimize cross talk) suffer from the high mechanical and thermal stress during packaging phase. As reported in [9], high-permittivity, k materials has been used in 45 nm technology to replace silicon SiO_2 as gate dielectric. The high-k materials could minimize the current leakage problem when the dielectric is made to become thinner to support physical scaling. However, the tendency of these materials to change their properties in high temperature is among the challenges need to be solved apart of adding new manufacturing process [19]. Several challenges are also reported in [1] such as appropriate tuning of metal work function, ensuring adequate channel mobility, gate stack integrity, and also the reliability of the material.

In summary, available materials do not satisfy the requirement to realize smaller CMOS devices. Moreover, the incapability to provide reliable characteristics as well as unprecedented unknown reliability mechanisms of new materials impact the development of CMOS scaling.

V. Power-Thermal Limitation

Since the supply voltage, V_{DD}, has not been scaling as fast as channel length, L, the power density has in fact been growing [15]. There are two types of power density dissipate by per unit area of integrated circuit (IC) chips namely *dynamic power density* and *static power density* [18]. Dynamic power density is dissipated when transistor is switched on. While static power density dissipation originates from the leakage source-drain current when transistor is switched off.

Figure 4 depicts both dynamic power density and static power density based on measured industrial data as mentioned in [15], at junction temperature of T_j = 25 °C. The former

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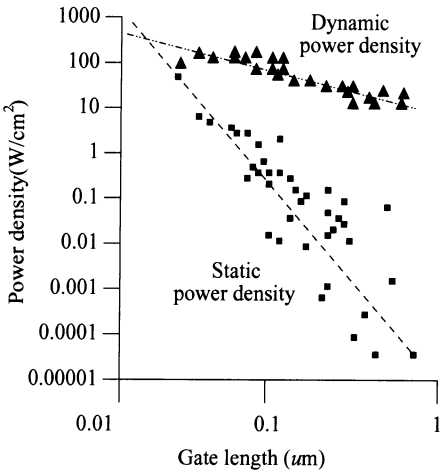

Fig. 4. Power density trend in CMOS [15].

found to be slightly more than 10 W/cm^2 at gate length of 0.9 μm, while, the latter found to has lower value (approximately 200000 times smaller for the same gate length). However, the power densities for both of them are becoming greater as gate length becomes smaller. It is more severe to the static power density where at the gate length of 20 nm, it will be equivalent to the dynamic power density. In the real operation, it turns to worst because the T_j is obviously more than 25 °C.

Power dissipation is proportional to the thermal heat. It means that, more heat is run away as greater power is dissipated. As reported in [21], a high performance microprocessor, which uses 10 KW of power, can draw heat at 1 KW/cm^2. For example, the power density of Intel® microprocessor is growing with the new generations. Before 1990s, the power density was below 10 W/cm^2, but when Pentium® family processor was introduced in 1990s, the power density increases exponentially. It is projected that the processor can be as hot as rocket nozzle when approaching the end of this decade if the current scaling trend is still continued without taking any prudence measures to tackle this power-thermal problem. As a result, Intel® canceled its 4 GHz Pentium®4 in 2001 due to heat dissipation problem. Consequently, they announced dual core processors.

In summary, although scaling materializes one billion of CMOS transistors in a single chip, the augmentation in integration contributes to the power and thermal problems. This negatively impacts the performance and reliability of CMOS transistor.

VI. Technology Limitation

CMOS transistors are basically patterned on wafer by means of lithography and masks. It means that the lithography technology is one of the main drives behind the transistor scaling. Ironically, the lithography processes cannot cope with the shrinking feature of CMOS transistors' layout. Lithography techniques such as proximity X-ray steppers and ion beam are limited by difficulties in controlling mask-wafer gap and uniform exposure of photoresists on wafer respectively. Another problem is the inability of polishing process to maintain the uniform thickness of wafer and reliable mask as mentioned in [14]. According to [20], patterning smaller feature than wavelength of light requires trade-off between complex, costly masks and possible design constraint. Figure 5 shows the evolution of mask from the 180 nm technology to the current technology [22].

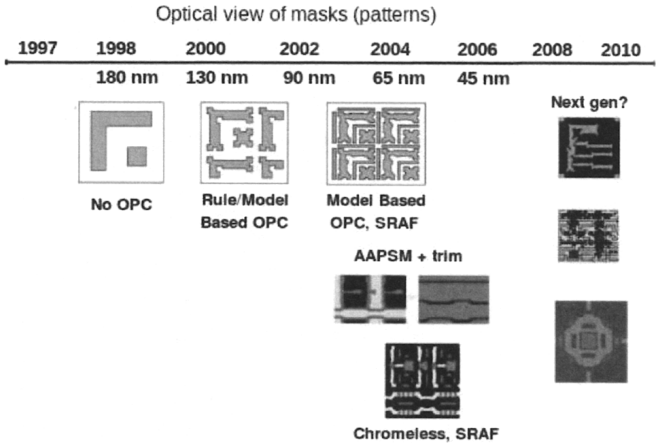

Fig. 5. Evolution of mask pattern [22].

For 180 nm technology, simple masks without optical proximity correction (OPC) are sufficient to pattern CMOS devices. When it comes to 130 nm technology, Rule/Model based OPC is already needed. As the technology shifts into below 100 nm, the masks become more complex and more advanced techniques are required. Moreover, it still a doubt how the future masks will be.

As reported in [22], patterning of features to 20 nm and below has been demonstrated by a variety of techniques. Newer techniques likes 248 nm radiation has been used to make 9 nm devices. However, the complexity of the processes involved may cause such approaches to be uneconomical. In addition, non-radiation patterning techniques (e.g. nanoimprint lithography) also appear very attractive but presently lack the investment needed to make them attractive for semiconductor IC manufacturing [22].

In summary, the current optical-based fabrication technology cannot support the resolution that are needed to pattern feature smaller CMOS sizes. Unless, this rudiment physic's law can be violated, this technology must be replaced to ensure smaller pattern can be fabricated.

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VII. Economic Limitation

Another biggest drive behind the downscaling is the economic consideration. The rising cost in semiconductor sector is basically contributed by the cost of production, and testing that escalating exponentially with time as the CMOS size is scaling down. As predicted by the National Institute of Standards and Technology (NIST), a new wafer foundary could cost approximately 25 billion dollar today, and will increase by one-fold in 2010 as depicted in Figure 6 [23].

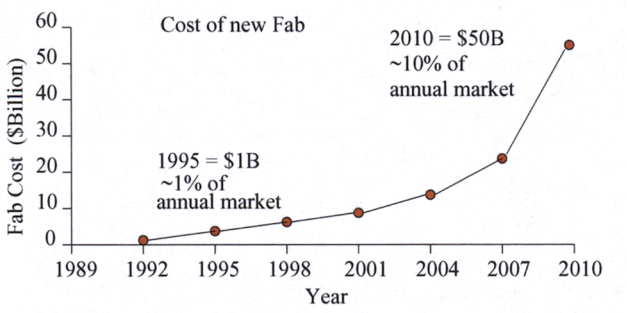

Fig. 6. Wafer foundry cost.

The cost explosion is also primarily contributed by the equipment cost, clean room facilities, and lithography process complexity [8],[24]. Traditional top down silicon based fabrication requires over 35 masks, and 700 steps for a 90 nm process [25]. The same trend is also stated in [26] for DRAM process fabrication. To gain sufficient profits, [27] states that on the average, DRAMs need 3000 to 5000 wafers per mask set, 1500 for a microprocessors, and 500 or less for ASICs and SOCs (i.e. for 130nm technology). Moreover, design revisions cause a hike in mask cost, and reduction in the number of wafer that can be produced in single mask set. The mask contribution is becoming the dominant factor in lithography costs, particularly as minimum feature sizes fall below the exposure wavelength. These problems lead to the combination of wafer production to the best equipped foundaries [28]. The alliances between companies and participation from universities and government that inject funding are also the strategy used to reduce the cost [4].

Smaller size circuit is vulnerable to hard and soft defects. These defective-prone circuits needs to be tested thoroughly in order to guarantee the required quality. However, more sophisticated test method will incur additional testing steps and time thus increasing test cost [29].

In summary, the success in future CMOS scaling requires a huge investment by semiconductor manufacturers. In spite of that, it is not clear if the high investment can guarantee higher profit margin due to increasing in cost of production operation and testing.

VIII. Potential Technologies Beyond CMOS

Because of numerous limitations of CMOS such as discussed in Section III to Section VII, it is expected that the transistor will end (or partially end) it service at the end of next decade [1]. Alternative devices are needed to be the complement or even the replacement to CMOS in future circuits. The nanodevices can be categorized into three classes [30]:

- *Electrical*-dependent nanodevices
  They are based either on *ballistic transport*, *tunneling* or on *electrostatic* phenomenon. In the case of ballistic transport the electrons travel without resistivity in a medium (material) [32]. In the case of tunneling, the electrons can pass through a potential energy barrier at some level of energy as results of a quantum-mechanical process [32]. In the case of electrostatic, the interaction of electrons happens with the presence of electric field [31]. Examples of nanodevices belong to this class are carbon nanotubes field-effect transistors (CNTFETs), semiconductor nanowire field-effect transistors (NWFETs), resonant tunneling diodes (RTDs), single electron junctions (SEJs), and electrical quantum dot cellular automata (EQCA) [31], [32].

- *Magnetic*-dependent nanodevices
  Magnetostatic and *spin transport* are the phenomena for the operation of the devices belonging to this class. In the case of magnetostatic, the magnetic dipole interactions are manipulated to carry the information [32]. In the case of spin transport, the spin polarized electrons transportation can be maintained by the magnetic field [32]. The example of nanodevices belong to this class are magnetic quantum dot cellular automata (MQCA) and spin field-effect transistors (spinFETs) [31], [32].

- *Mechanical*-dependent nanodevices
  Restructuring of conductive polymers is the phenomenon for this category. The structure of the polymer moves or changes when activated by input sources [32]. These nanodevices have been utilized in molecular memory and FPGA [30].

These nanodevices possess some advantages compared to CMOS devices. CNTFETs have an extraordinary mechanical strength, low power consumption, better thermal stability, and higher resistance to electromigration [31]. The advantages of NWFETs over CMOS are similar to carbon nanotube based devices [31], plus the ability to operate at high speed, produces saturated current at low bias voltage, and the potential to behave as either active or passive devices in single nanowire [32]. The benefits of using RTDs instead of CMOS in electronic circuits are related to faster operation, reduced component count per transistor, higher circuit density, and lower power consumption [31]. The avail of SEJs compared to CMOS transistors are better scalability, faster operation, and less power consumption [31], [32]. EQCA and MQCA exhibit

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greatness in low power dissipation, non-volatility, and reconfigurability [32]. SpinFETs have the advantages of high power gain, small off-current, low power consumption, tunable, high operating speed, nonvolatile, and better noise margin compared to CMOS [31], [32]. The extremely small-size molecular electronic devices, which are low power, scalable, and can be self assembled [32].

IX. Conclusion

In this paper we have discussed the main challenges faced by CMOS technology. The challenges are addressed from different perspectives; physical, material, power-thermal, technological, and economical. We have also presented alternative devices that are potentially able to overcome the limitation in CMOS technology. At present, the research of these emerging non-CMOS nanodevices is still in its infancy phase. Therefore, researchers are urged to continue exploring and inventing these new, high-performance, and cost-effective non-CMOS nanodevices before the extinction of CMOS.

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