FinFET 3D Transistor & the Concept Behind It

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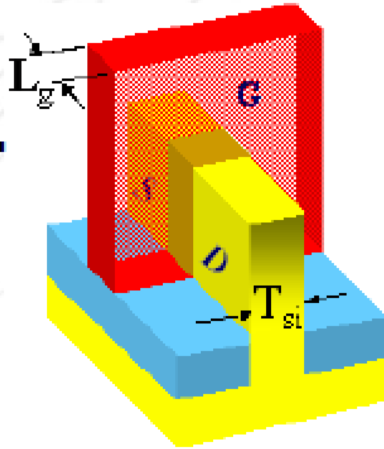
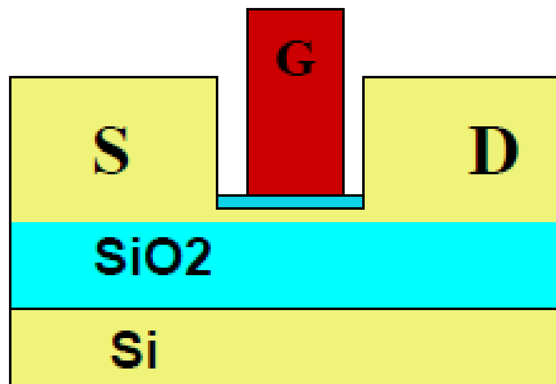
- Intel will use 3D FinFET at 22nm
- Most radical change in decades
- There is a competing SOI technology

New MOSFET Structures

FinFET

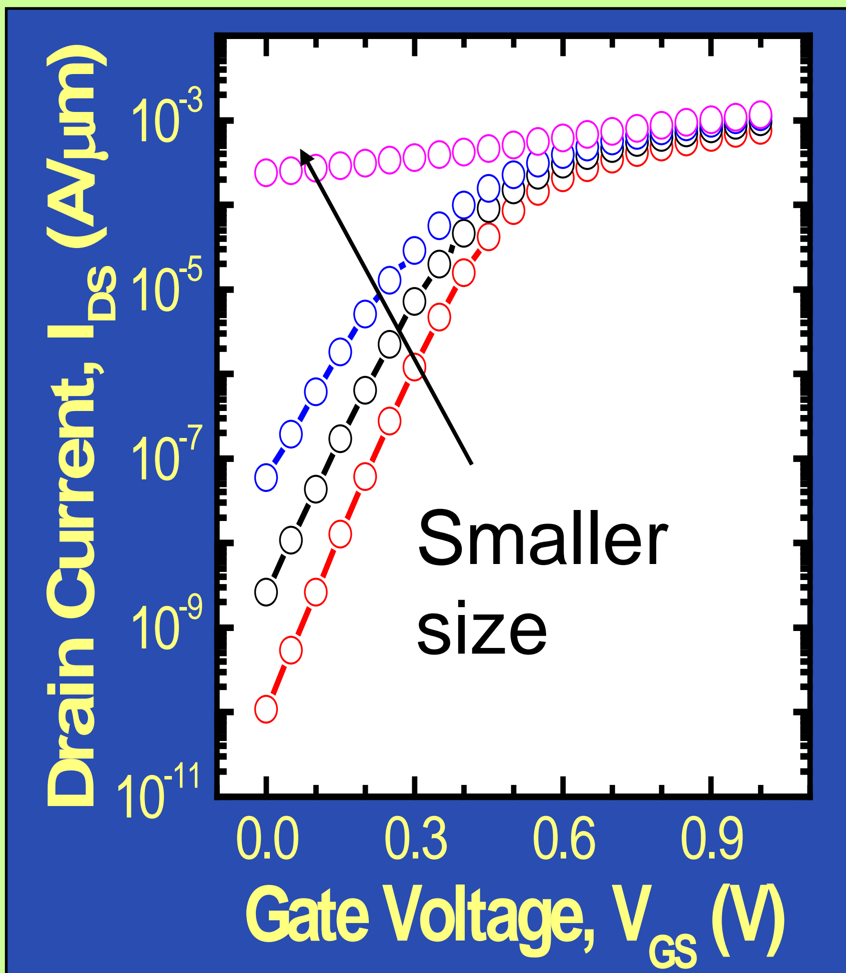


UTBSOI



Ultra Thin Body SOI

Good Old MOSFET Nearing Limits



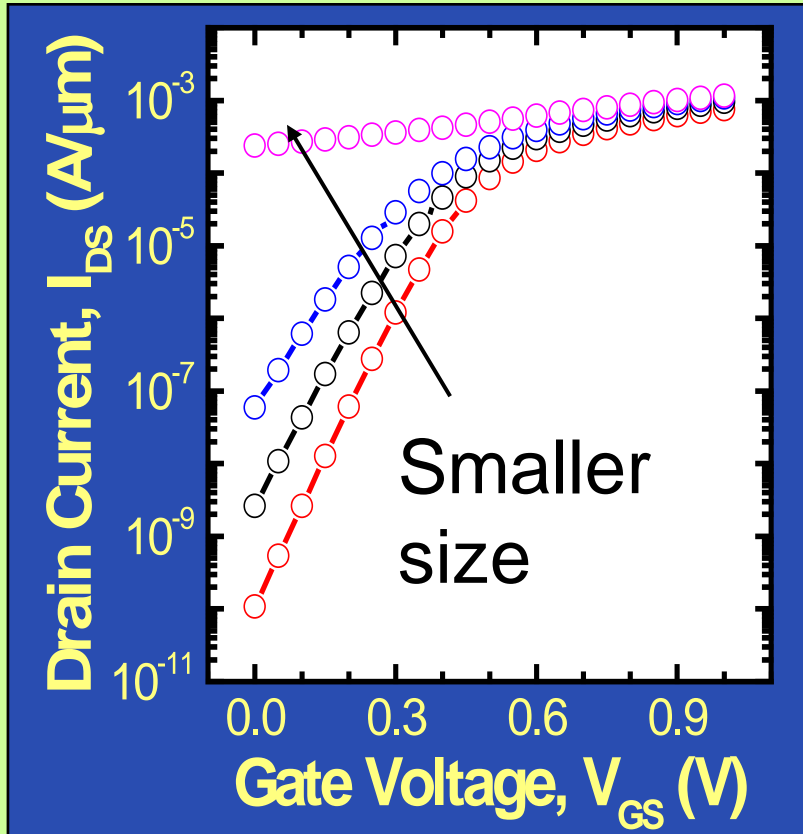
- Vt, S, Ioff are bad & sensitive to Lg
- Dopant fluctuations.

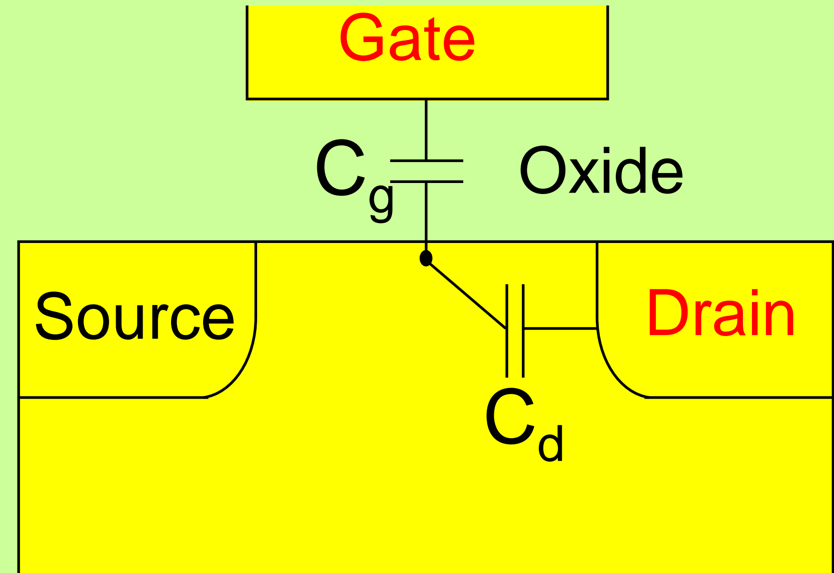
Requiring

- higher Vt, Vdd, and power consumption
- higher design cost

Finally painful enough for change.

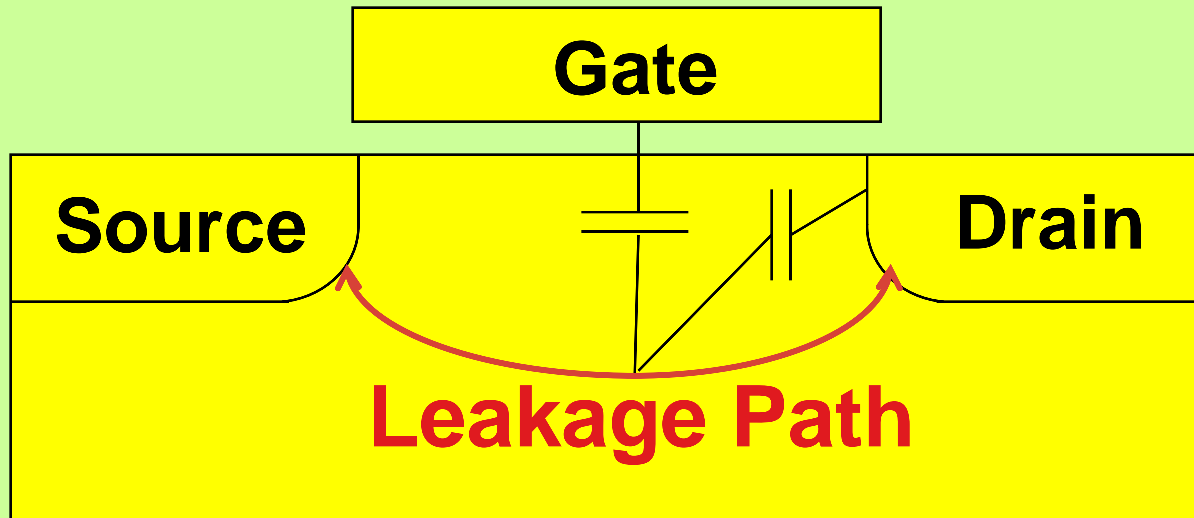
Why V_t Variation & Swing are So Bad





MOSFET becomes "resistor" at very small L – Drain competes with Gate to control the channel barrier.

Making Oxide Thin is Not Enough

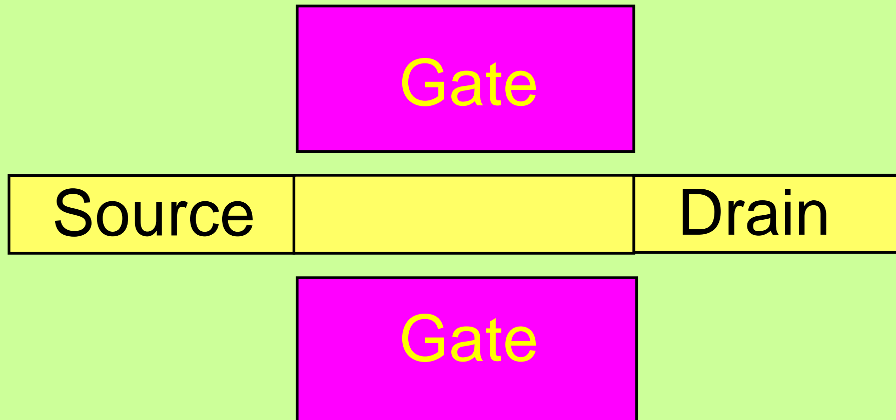


Gate cannot control the leakage current paths that are far from the gate.

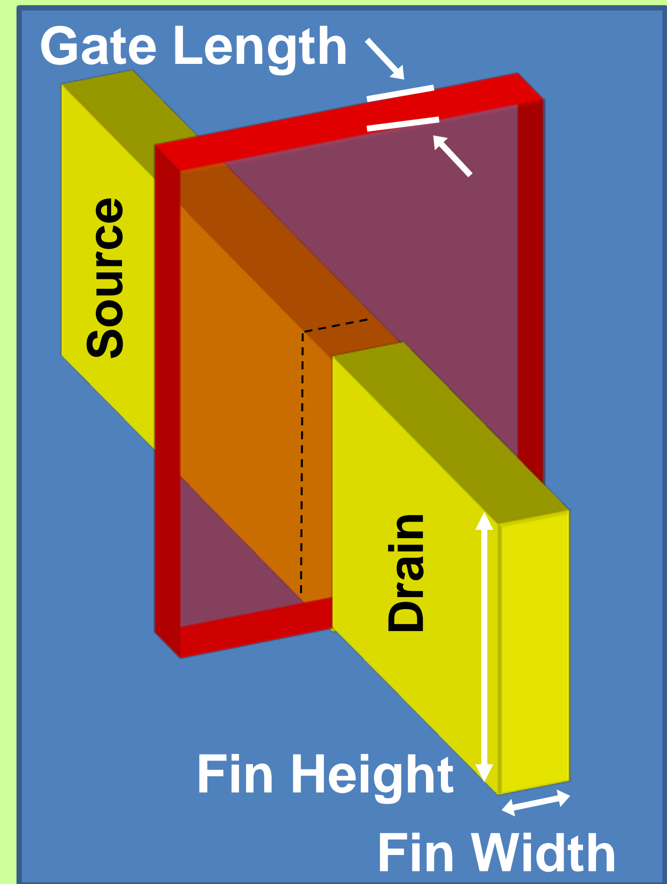
C.Hu,"Modern Semicon. Devices for ICs" 2010, Pearson

One Way to Eliminate Si far from Gate

A thin body controlled by gate from more than one side.



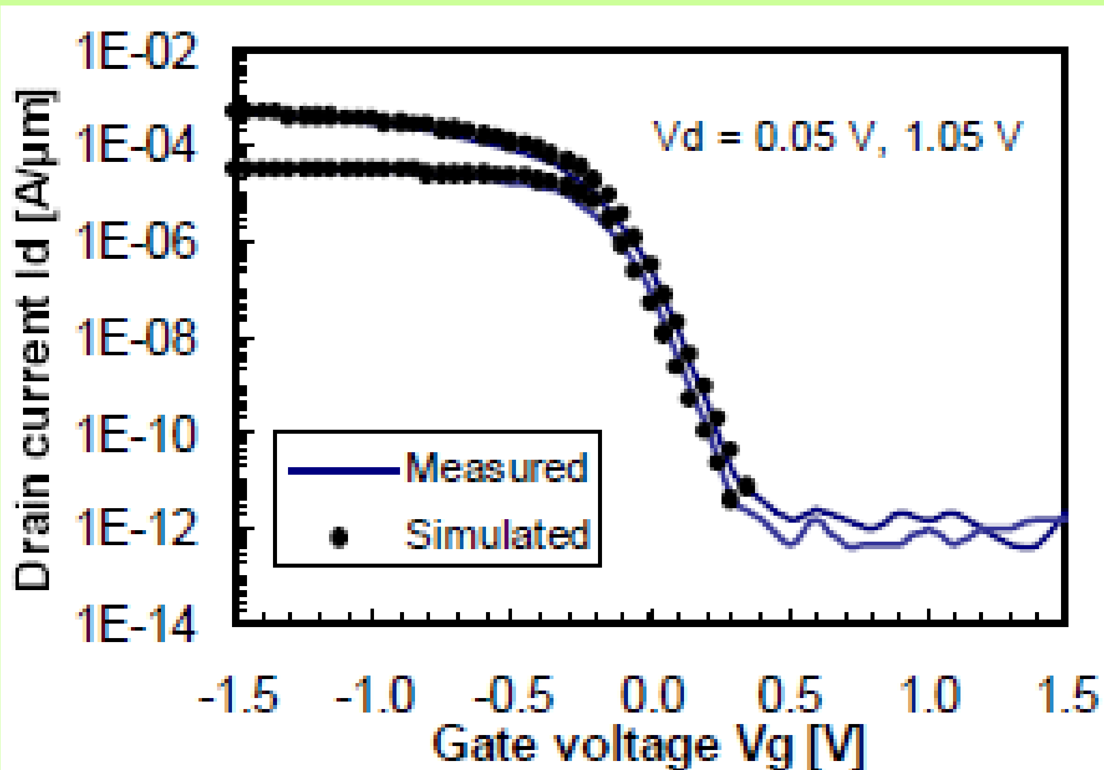
FinFET body is a thin fin

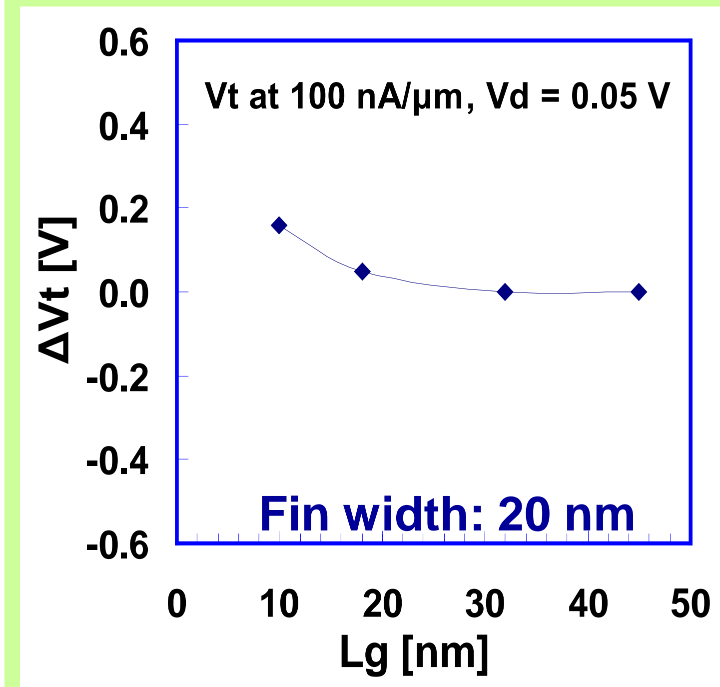


N. Lindert et al., DRC paper II.A.6, 2001

FinFET- 1999

Undoped Body. 30nm etched thin fin. Vt set with gate work-function.



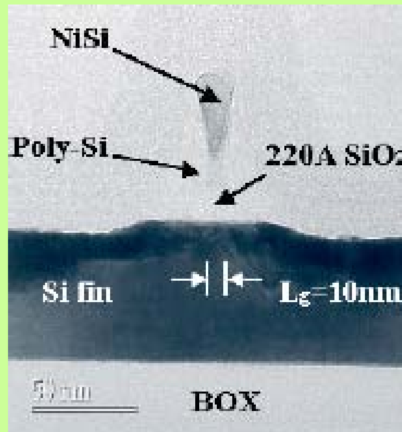


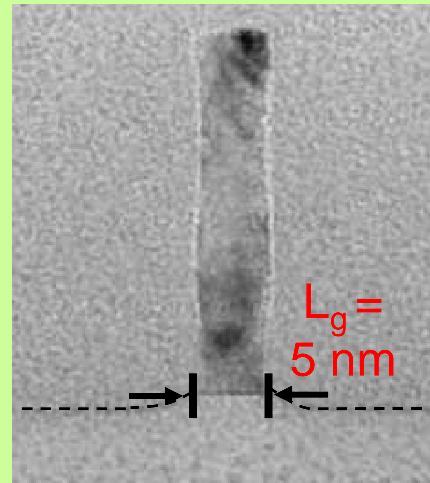
X. Huang et al., IEDM, p. 67, 1999

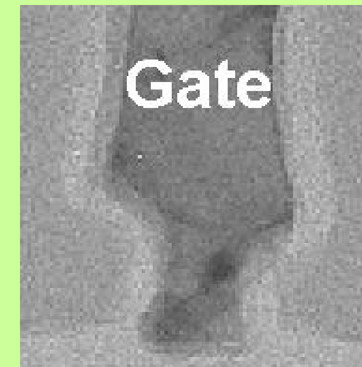
DARPA Device Group Meeting 1999

FinFET is "Easy" to Scale

10nm Lg AMD 2002 IEDM	5nm Lg TSMC 2004 VLSI Symp	3nm Lg KAIST 2006 VLSI Symp





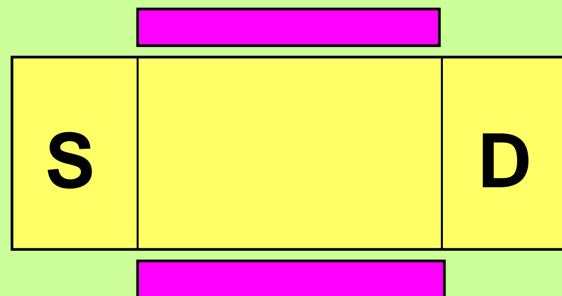


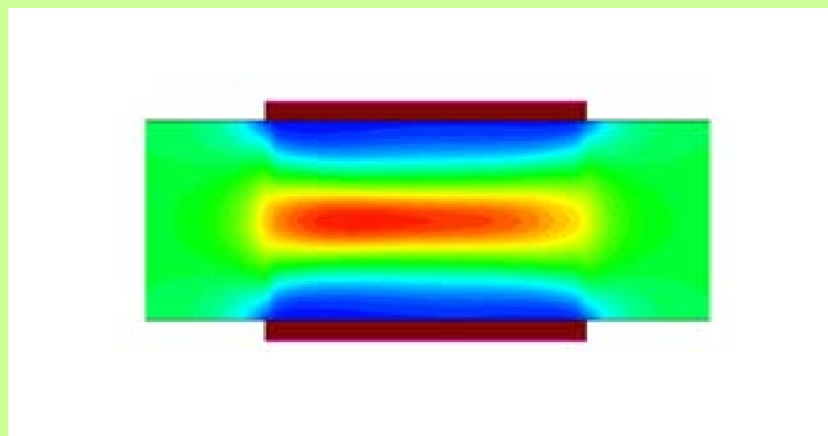
Leakage is well suppressed if

Fin thickness =or< Lg

- Thin fin and gate can be made with the same lithography and etching tools.

FinFET Leakage Path





Body thickness is the new scaling parameter.

C.Hu,"Modern Semicon. Devices for ICs" 2010, Pearson

Two Improvements to FinFET

Original FinFET had thick oxide on fin top & used SOI for process simplicity.

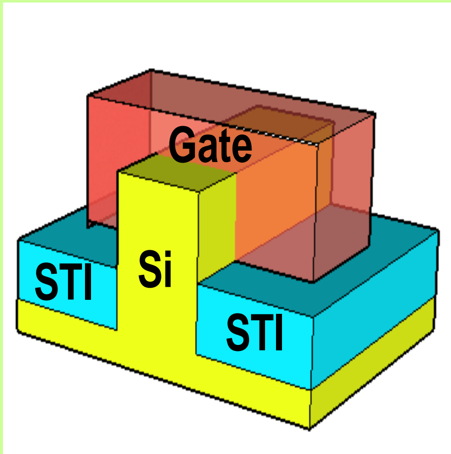
- 2002 FinFET with thin oxide on fin top.

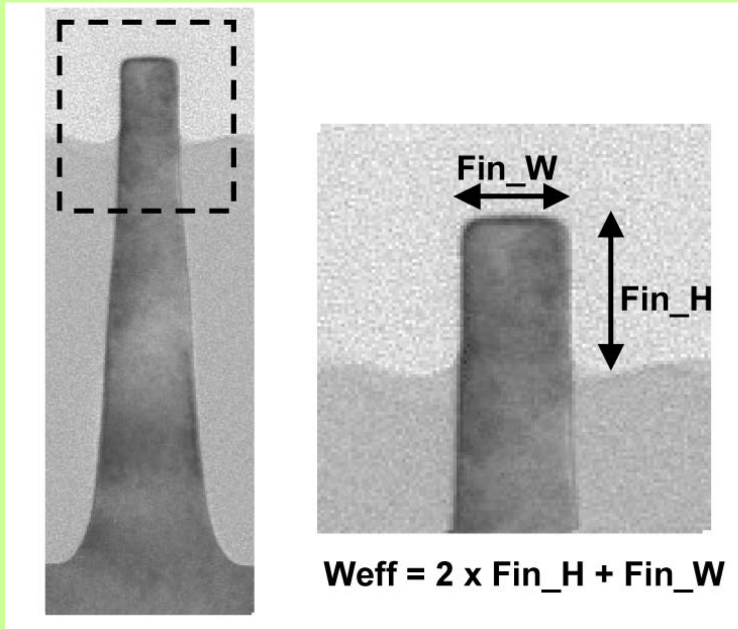
F.L.Yang et al. (TSMC) 2002 IEDM, p. 225.

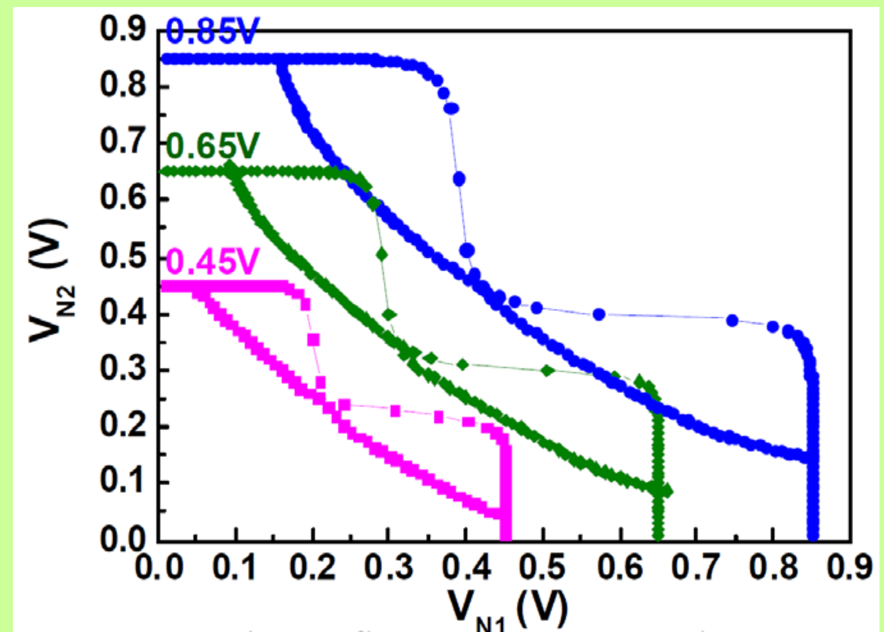
- 2003 FinFET on bulk substrate.

T. Park et al. (Samsung) 2003 VLSI Symp. p. 135.

State-of-the-Art FinFET





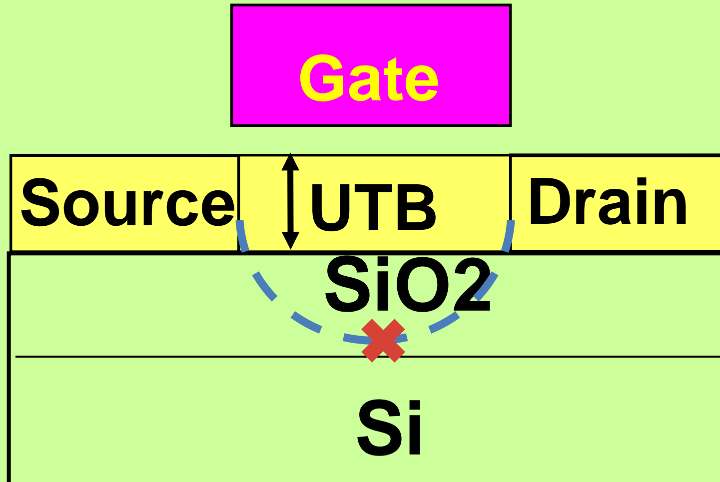


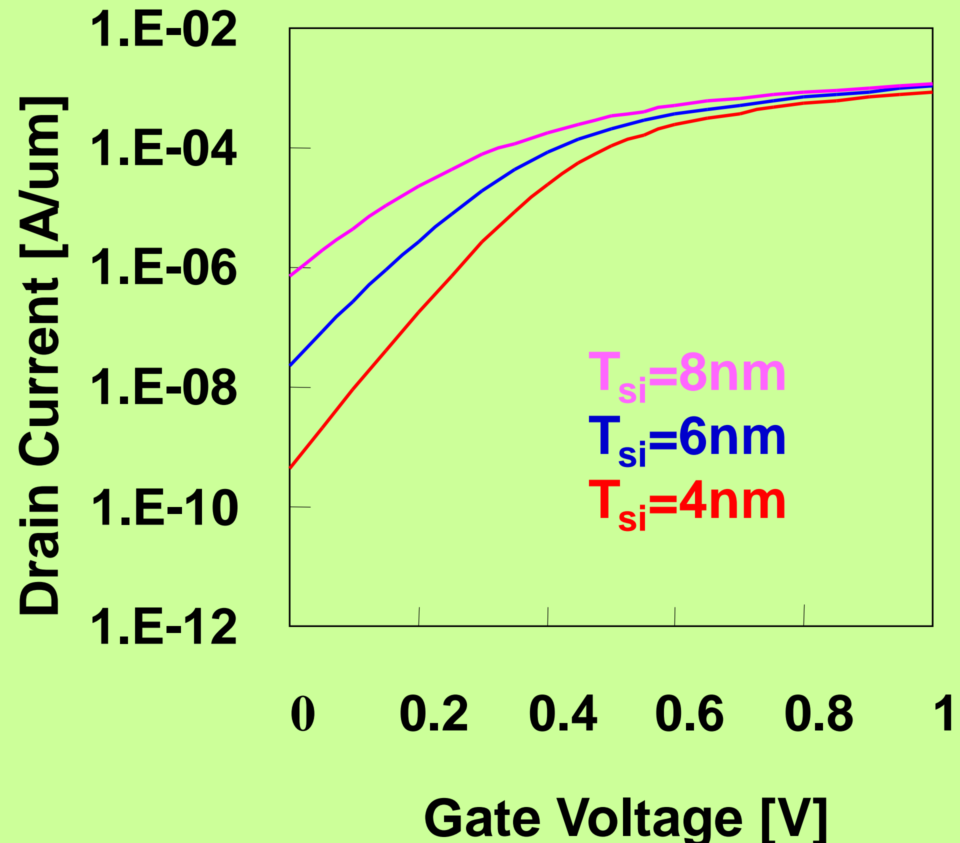
20nm Hi Perf
C.C. Wu et al.,
2010 IEDM

2nd Way to Eliminate Si far from Gate

Ultra-thin-body SOI (UTB-SOI) →

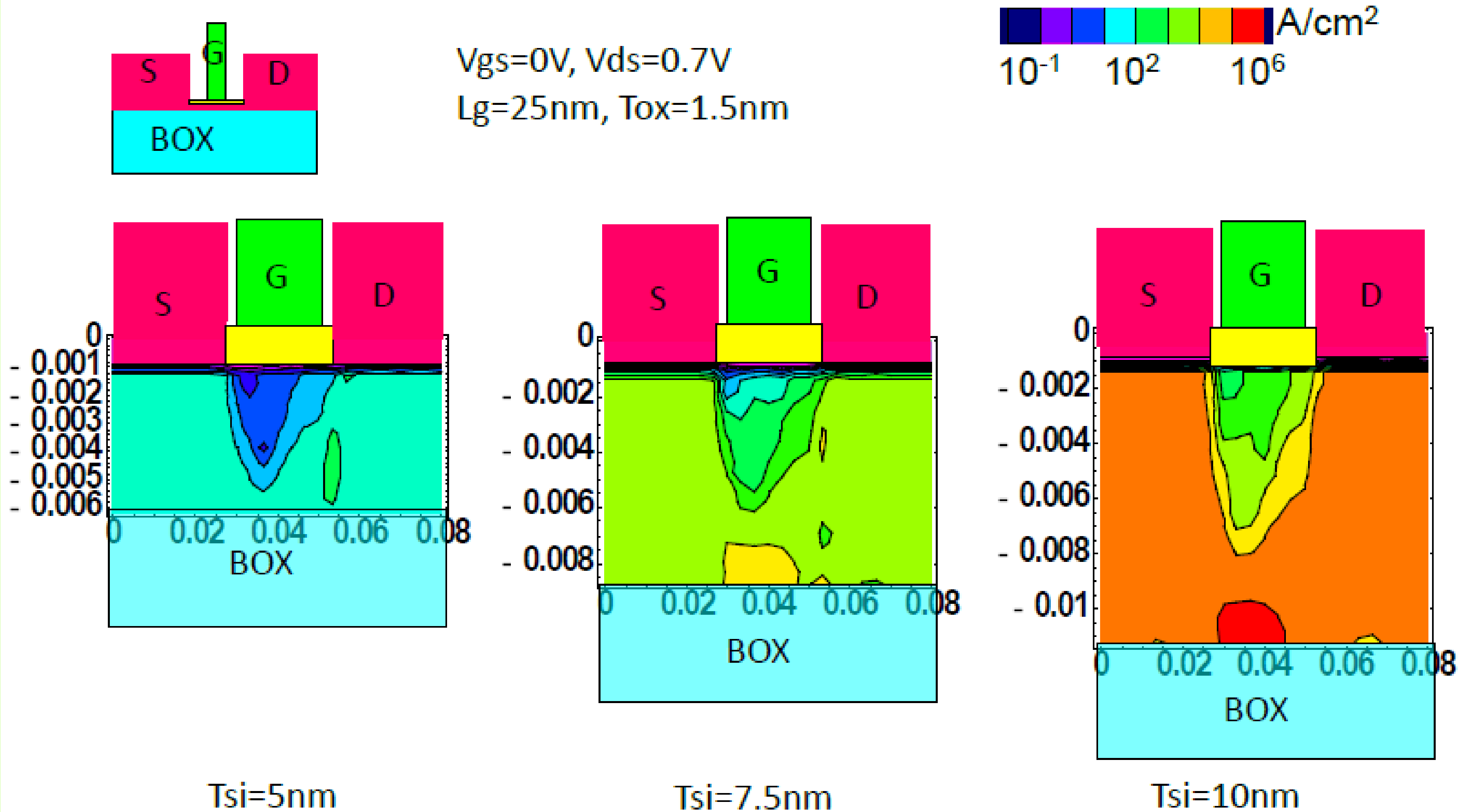
No leakage path far from the gate.





Y-K. Choi, IEEE EDL, p. 254, 2000

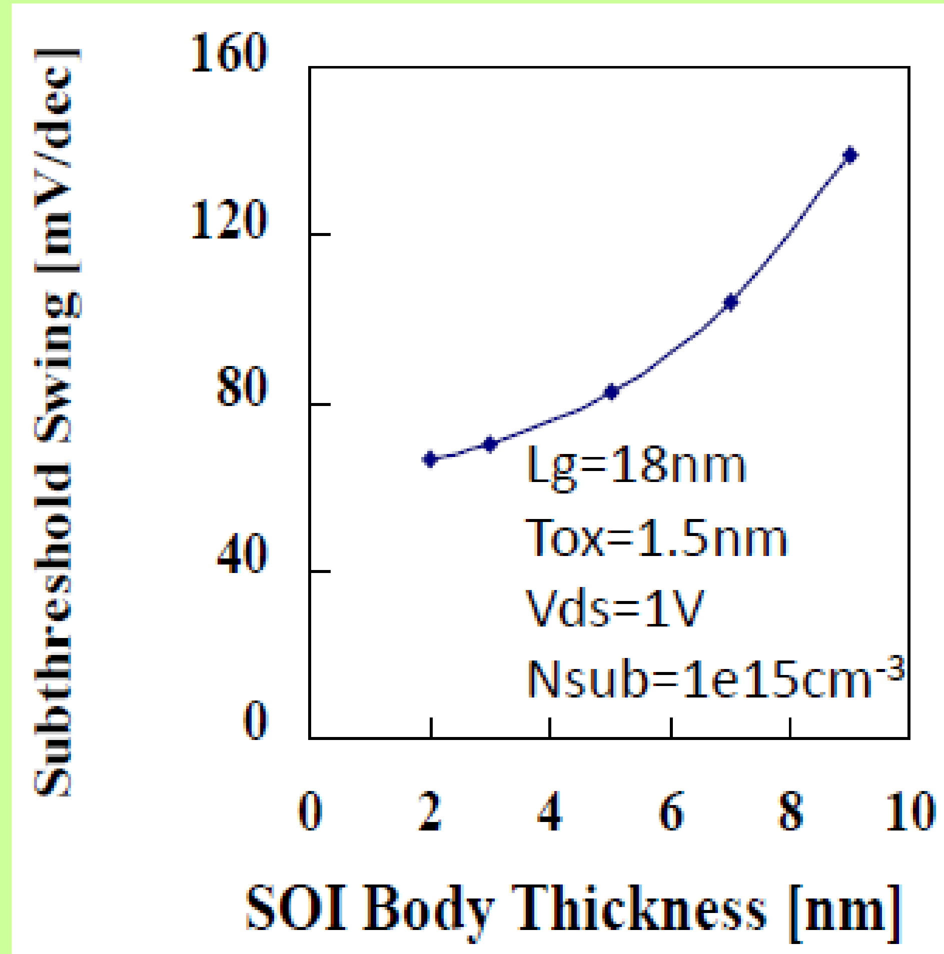
Most Leakage Flows >5nm Below Surface



Y-K. Choi et al., IEEE Electron Device Letters, p. 254, 2000

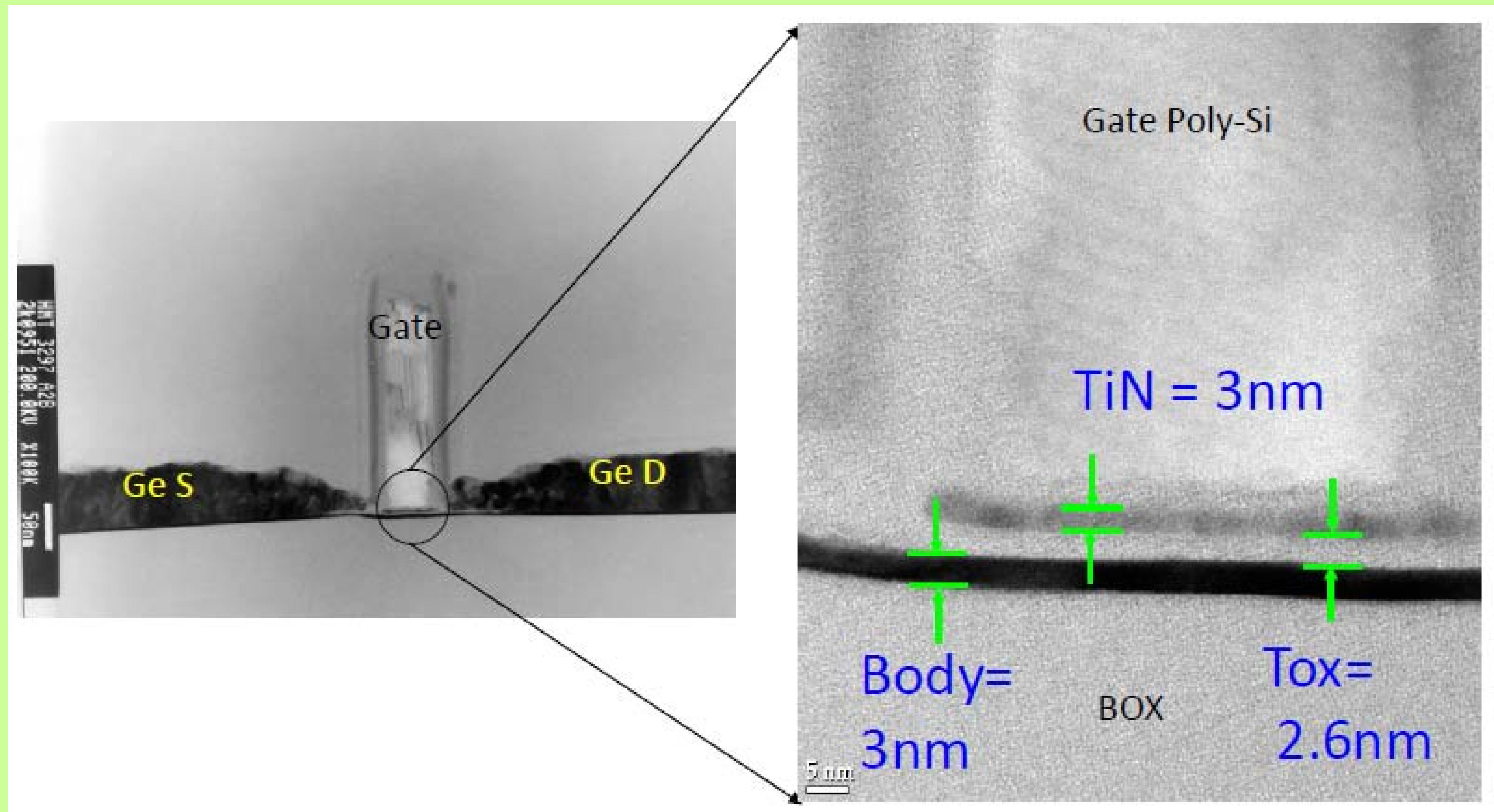
Silicon Body Needs to be <Lg/3

For good swing and device variation



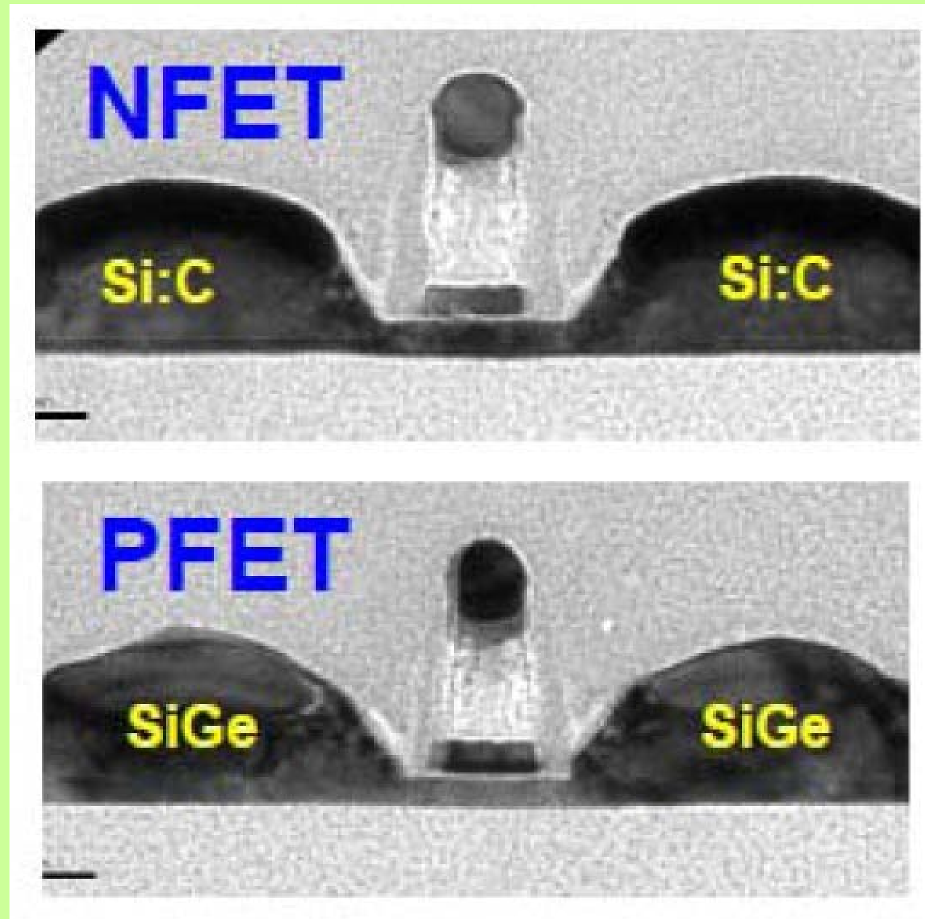
Y-K. Choi et al., IEEE Electron Device Letters, p. 254, 2000

UTB-SOI
3nm Silicon Body, Raised S/D



Y-K. Choi et al, VLSI Tech. Symposium, p. 19, 2001

State-of-the-Art 5nm Thin-Body SOI



ETSOI, IBM

K. Cheng et al, IEDM, 2009

Both Thin-Body Transistors Provide

- Better swing.
- S & Vt less sensitive to Lg and Vd.
- No random dopant fluctuation.
- No impurity scattering.
- Less surface scattering (lower Eeff).

- Higher on-current and lower leakage
- Lower Vdd and power consumption
- Further scaling and lower cost

Similarities between FinFET & UTBSOI

Device Physics

- Superior S, scalability and device variations

-use body thickness as a new scaling parameter
-can use undoped body for high μ and no RDF

History

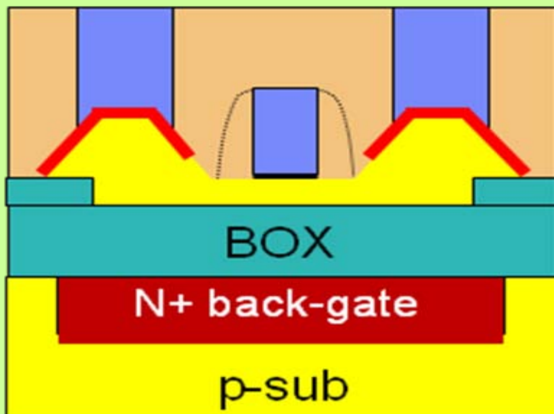
- 1996: UC Berkeley proposed both to DARPA as “25nm Transistors”.
- 1999: demonstrated FinFET
  2000: demonstrated UTB-SOI
- Since 2001: ITRS highlights FinFET and UTBSOI

Main Differences

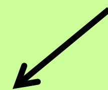
• FinFET body thickness ~Lg. Investment by fab.
UTBSOI thickness ~1/3 Lg. Investment by Soitec.

• FinFET has clearer long term scalability.
UTBSOI may be ready sooner than FinFET for some companies.

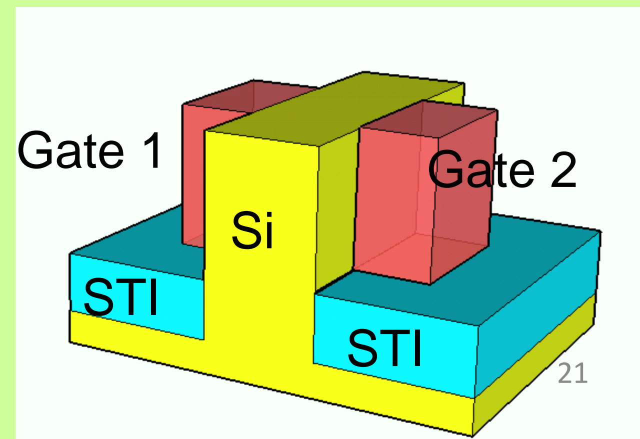
• FinFET has larger Ion.
UTBSOI has a good back-gate bias option.



UTBSOI



FinFET



What May Happen

- FinFET will be used at 22nm by Intel and later by more firms to <10nm.
- Some firms may use UTBSOI to gain market from regular CMOS at 20/18/16nm.

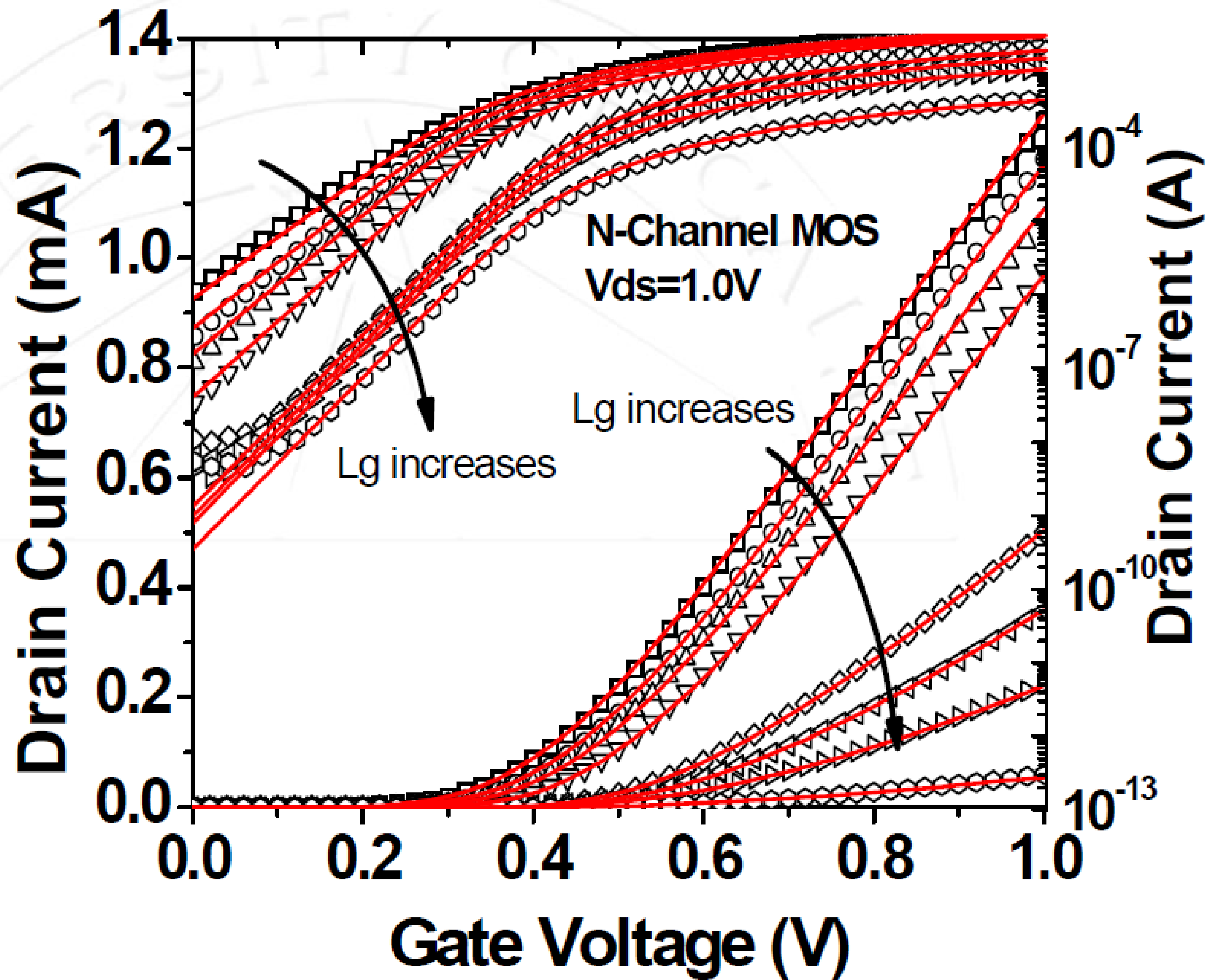
If so, competition between FinFET and UTBSOI will bring out the best of both.

BSIM SPICE Models

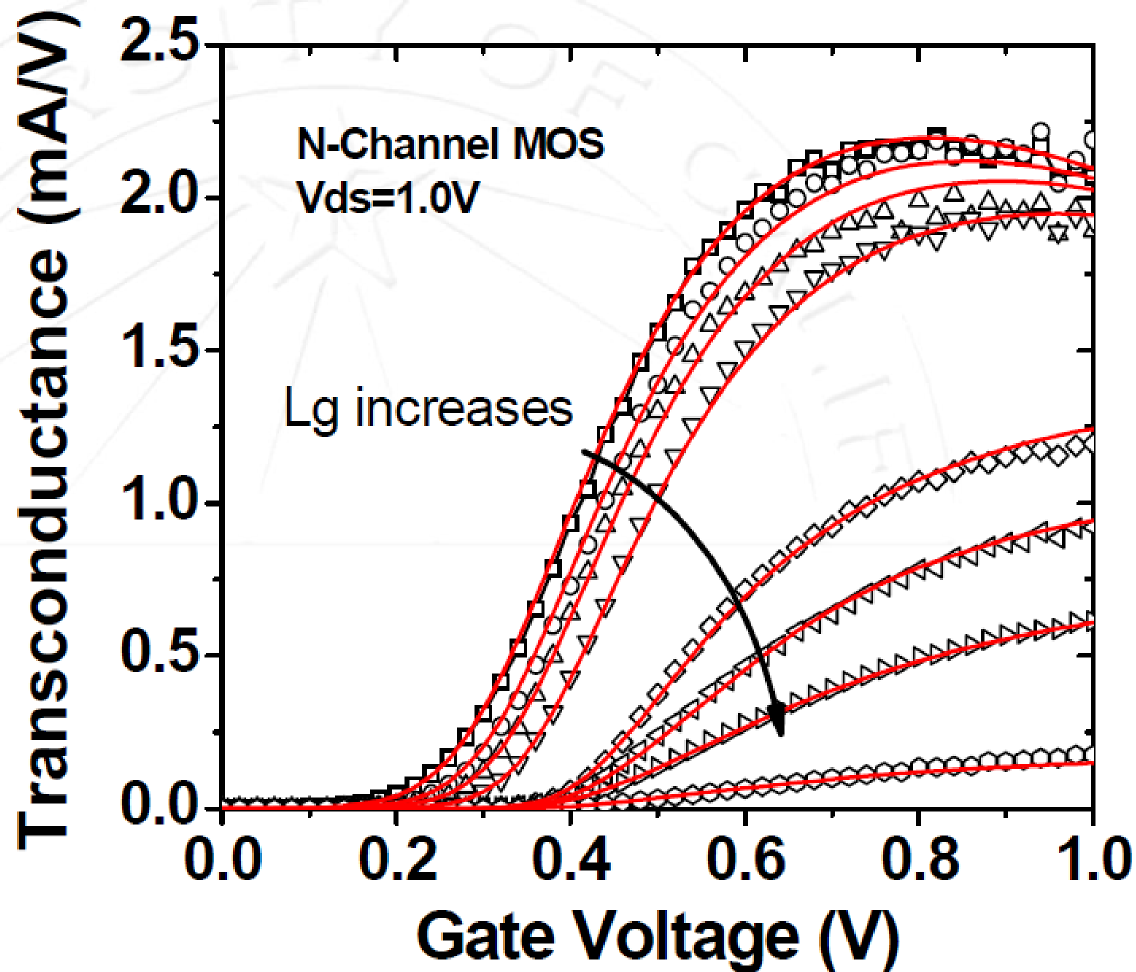
Berkeley Short-channel IGFET Model

- **1997: became first industry standard MOSFET model for IC simulation**
- **BSIM3, BSIM4, BSIM-SOI used by hundreds of companies for design of ICs worth half trillion dollars**
- **BSIM models of FinFET and UTBSOI are available – free ☺**

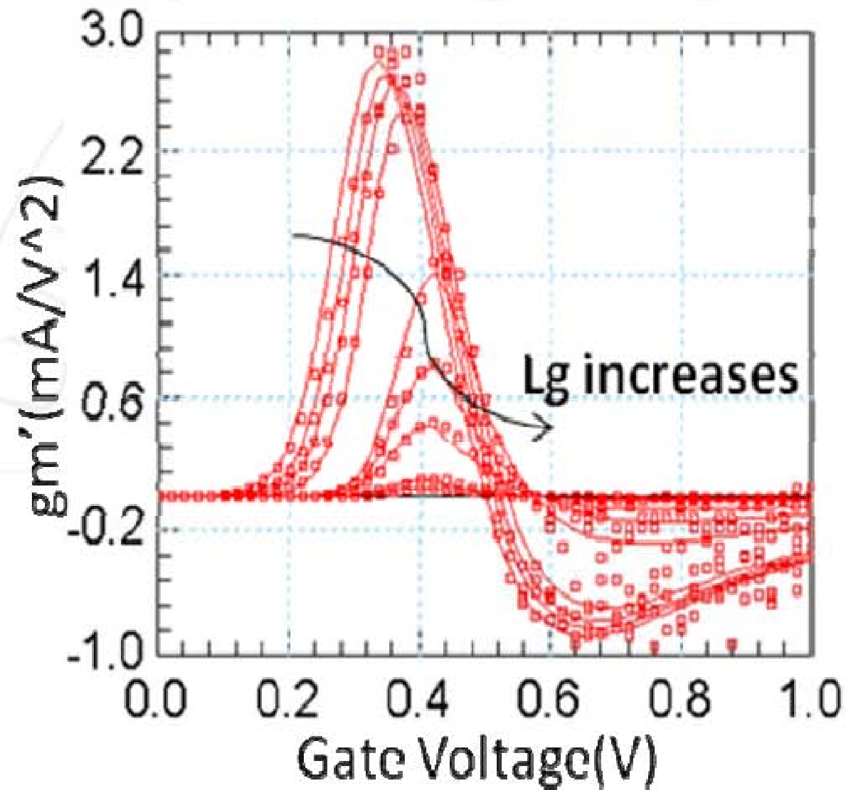
Global fitting with 30nm-10um FinFETs

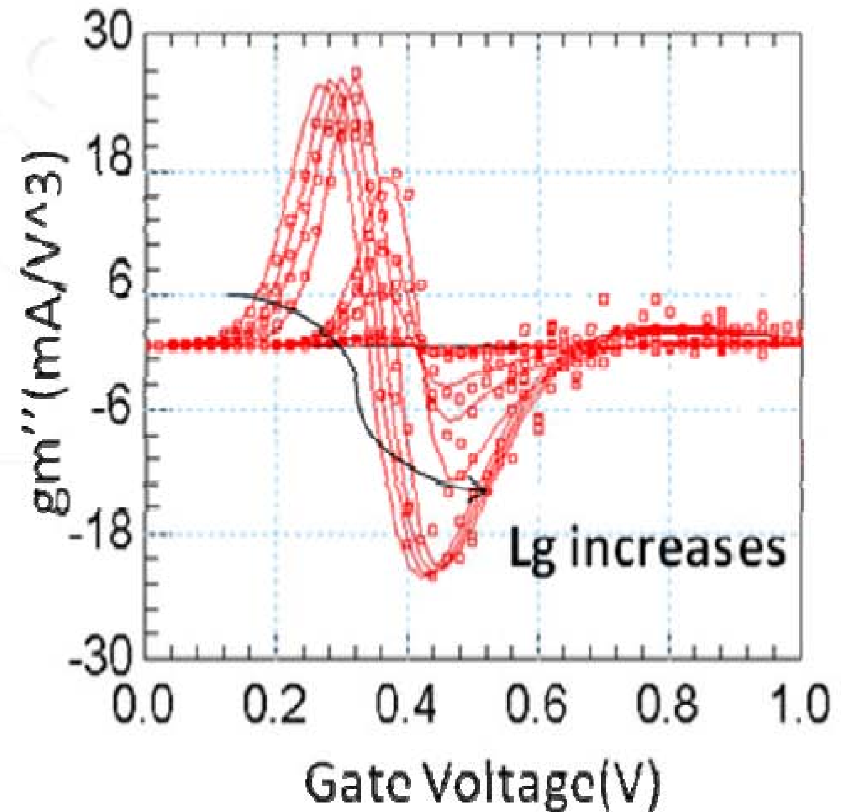


Global fitting with 30nm-10um FinFETs

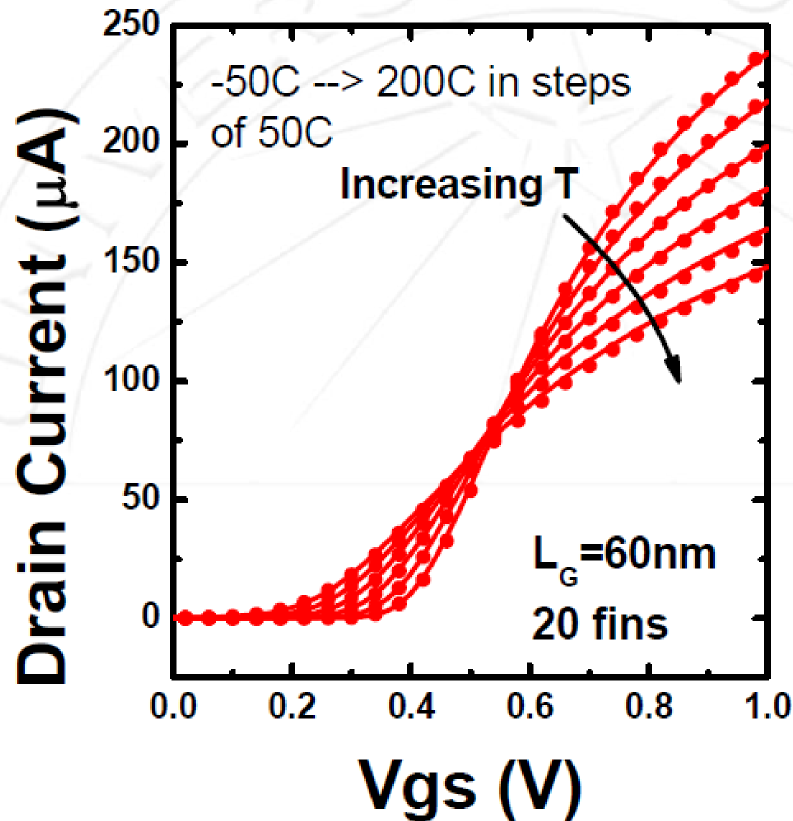


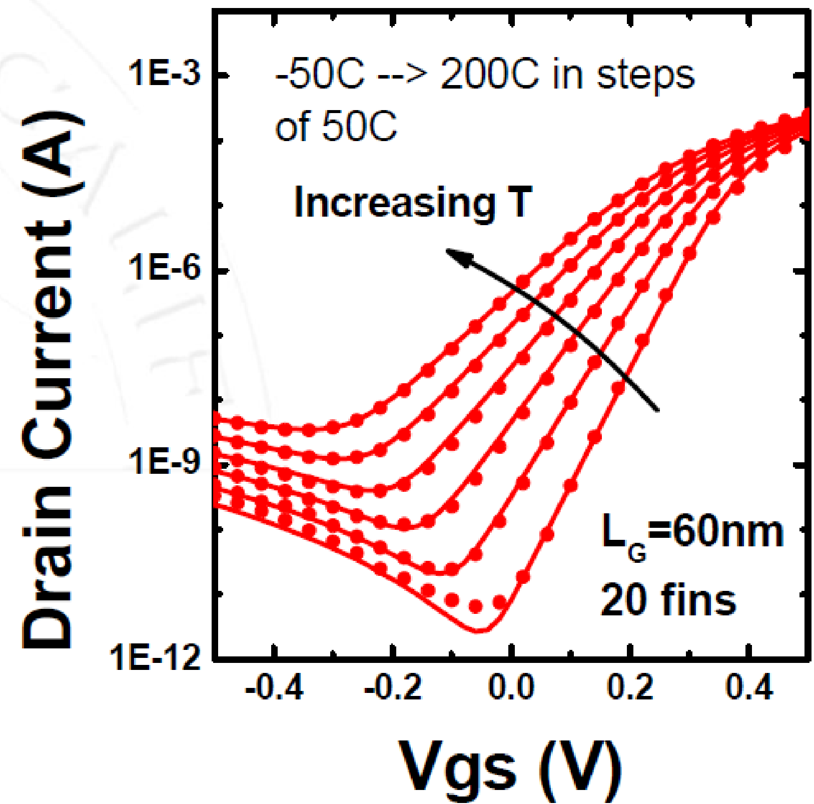
Global fitting with 30nm-10um FinFETs





Temperature Model Verified for FinFET





Summary

- **FinFET and UTB-SOI allows lower Vt and Vdd → Lower power.**
- **Body thickness is a new scaling parameter → Better short channel effects to and beyond 10nm.**
- **Undoped body → Better mobility and random dopant fluctuation.**
- **BSIM models of FinFET and UTBSOI are available – free ☺**