Introduction to Special issue on Reconfigurable computing and FPGAs

During the last three decades, FPGA technology has quickly evolved to become a major subject of research in computer and electrical engineering as it has been identified as a powerful alternative for creating highly efficient computing systems. FPGA devices offer substantial performance improvements when compared against traditional processing architectures via custom design and reconfiguration capabilities.

This special issue of *Microprocessors and Microsystems* presents advances of current research and development in aspects related to Reconfigurable Computing and FPGA devices. It contains a total of five extended versions of selected papers presented at the 2013 International Conference of Reconfigurable Computing and FPGAs, ReConFig 2013, which was held in Cancun, Mexico, during December 9–1, 2013. All papers were peer reviewed to ensure that they are presented with the breadth and depth expected from this high quality journal.

In the paper entitled "SAccO: An implementation platform for scalable FPGA accelerators", Weinhardt et al. presents a framework for implementing data-intensive applications using scalable and portable reconfigurable hardware accelerators. As an alternative to using "reconfigurable supercomputers", SAccO is based on standard PCs and PCI-Express extension cards featuring Field-Programmable Gate Arrays (FPGAs) and memory. Authors exploit task-level parallelism by manually partitioning applications into several parallel processes using the SAccO communication API for data streams. If an FPGA accelerator is present, the same API calls transfer data between the PC's CPU and the FPGA. Then, the processes implemented in hardware can exploit instruction-level and pipelining parallelism as well. The framework also comprises a new method to automatically select a task's optimal degree of parallelism on an FPGA for a given hardware platform.

In the paper entitled "ASTRO: Synthesizing application-specific reconfigurable hardware traces to exploit memory-level parallelism", Lin et al. address the problem of how to cost-effectively synthesize application-specific hardware constructs that fully exploit memory-level parallelism when using integrated CPU + FPGA hybrid platforms. Authors propose a FPGA-based embedded computer architecture, named ASTRO (Application-Specific Hardware Traces with Reconfigurable Optimization), that can (1) perform dynamic memory analysis to maximally extract the target application's instruction, loop and memory-level parallelism for performance enhancement, (2) synthesize highly efficient accelerators that enable parallelized memory accesses, and therefore (3) accomplish effective data orchestration by utilizing the capabilities of modern FPGA devices: abundant distributed block RAMs and reprogrammability.

Similarly, in the paper entitled "FPGA-GPU communicating through PCIe", Thoma et al. address the interaction and benefits of coupling GPUs and FPGAs with a general purpose processor (CPU). Authors present an implementation of a GPU-FPGA direct communication. The transfer is triggered by a central CPU but managed by the FPGA, in a DMA-like manner. Performance results for different hardware setups are presented and compared. The various measurements demonstrate achieved data rates that are close to the theoretical maximum, with some interesting outliners, and a very low interfacing latency.

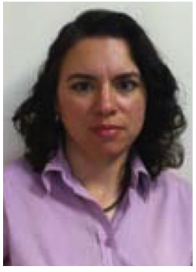
In the paper entitled "Processor arrays generation for matrix algorithms used in embedded platforms implemented on FPGAs", Perez-Andrade et al. address the problem of efficient FPGA-based hardware implementation of matrix algorithms. They present an approach for efficient data memory accesses and data transferring for feeding a processor array, as well as support for solving problems independently of their size and limited only by the FPGA available resources. The proposed approach was validated by generating processor arrays for three different matrix algorithms used in digital signal processing applications.

Finally, in the paper entitled "Hardware/Software Co-design of Physical Unclonable Function based Authentications on FPGAs", Aysu and Schaumont propose Physical Unclonable Functions (PUFs) constructions that are tightly integrated into the design of a micro-processor. The proposed PUFs are a collection of time-to-digital converters that are integrated into the custom instruction or memory-mapped interface of a processor. Therefore, the processor can issue the PUF challenges and collect the associated responses using instruction executions. Authors describe the design, implementation, and the performance analysis details of such hardware/software co-designed authentication mechanisms on FPGAs. Measurements reveal that the proposed solutions can authenticate trillions of devices and provide better performance than the ring oscillator based alternative.

It is our pleasure to express our sincere gratitude to all who contributed in any way to produce this Special Issue. We would like to thank all the reviewers for their valuable time and effort in the review process, and to provide constructive feedbacks to authors. We thank all authors who contributed to this Special Issue for submitting their manuscript and sharing their latest research results. We hope that you will find in this Special Issue a valuable source of information to your future research.

René Cumplido holds a BSc degree in Computer Systems from the Queretaro Institute of Technology, Mexico, a MSc in Electrical Engineering from the CINVESTAV, Mexico, and a PhD Electrical Engineering from Loughborough University, UK. Since 2002, he is a professor at the Computer Science Department at INAOE in Puebla, Mexico. His research interests are Reconfigurable Computing for DSP and Digital Communications, FPGA Technologies and Custom Architectures for Scientific Computing. He is co-founder and Chair of the ReConFig international conference and founder editor-in-chief of the International Journal of Reconfigurable Computing. He also serves as associate editor of several international journals.

Eduardo de la Torre got all his degrees from the Technical University of Madrid (Spain), M.Eng in 1989 and Ph.D. in 2000. His research has been centered in the last years in reconfigurable systems and architecture design for FPGA-based embedded systems. In the last five years he has published more than 30 contributions in Conferences and Journals on the topic of reconfigurable systems, targeting embedded and resource or energy restricted systems, but providing features such as autonomy, self-reconfiguration, self-adaptation and self-healing. Presently he is an Associate Professor in the area of Electronic Technology at the Technical University of Madrid.



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