Testing of Level Shifters in Multiple Voltage Designs

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Abstract— **The use of multiple voltages for different cores is becoming a widely accepted technique for efficient power management. Level shifters are used as interfaces between voltage domains. Through extensive transistor level simulations of resistive open, bridging and resistive short faults, we have classified the testing of level shifters into PASSIVE and ACTIVE modes. We examine if high test coverage can be achieved in the PASSIVE mode. We consider resistive opens and shorts and show that, for testing purposes, consideration of purely digital fault effects is sufficient. Thus conventional digital DfT can be employed to test level shifters. In all cases, we conclude that using sets of single supply voltages for testing is sufficient.**

I. Introduction

With increasing demand for power-aware consumer products, energy-efficient operation has become an important design objective, particularly in battery-operated mobile applications. Most applications do not always require the peak performance, therefore, in multiple voltage design, the system's voltage/frequency (V/F) setting may be dynamically varied according to the performance requirements. This can be taken a step further with Dynamic Voltage scaling (DVS), which has been implemented in several contemporary embedded microprocessors, such as Intel's XScale [1] and Transmeta's Crusoe [2]. In a previous paper [3], we looked at the general concept of testing multi-voltage circuits. Here, we look in detail at one of the important circuit components in such system, the logic-swing level shifter. In a multiple voltage system, level shifters are required between the core blocks and between the core and I/O circuits.

In general, a level shifter is built using specially characterized standard cells. Tran [4] has proposed two different types of level shifter: Contention mitigated level shifters (CMLS); and Bypassing enabled level shifters (BELS). Khan [5] has proposed single supply level shifters for multi-voltage systems with low leakage current and also capable of shifting at a high frequency.

This paper attempt to answer two key questions. Can we test a level shifter as a digital circuit using conventional Design-For-Test(DFT) techniques? Can we test the level shifters using one or set of single voltages (at one time)? In part II of the paper, we show cases whereby normally insensitive input vectors such as (1,1) for a bridging fault become sensitive with the inclusion of level shifters in the circuit. Part III of the paper studies the ability for the level shifters to propagate the fault effect. Part IV of this paper investigates the feasibility of using a single supply voltage to detect the faults in level shifters. Although, by definition, level shifters are designed to operate between two voltage domains, it would be easier if tests could be performed using a single supply voltage. This would reduce the complexity of the Design-For-Test(DFT) architecture.

II. Level Shifters in the Presence of Resistive bridging faults

In previous works [6], [7], it has been noted that bridging defects are dormant as long as both driving signals are the same. However, in a multi voltage chip, the driving signals can originate from different cores that are operating at different supply voltages. If the level shifter is defective, there is the possibility that the output signal from the level shifter is misinterpreted. To demonstrate this, we have conducted simulations in which two defects are injected: a malfunctioning level shifter and a bridging fault. In these simulations we have overruled the classic Single Fault Assumption (SFA).

Figure 1 shows the circuit model used in our study. The level shifters' function is to bring up the voltage signal from VDDL (0.85V) to VDDH (1.7V). R_bridge is the bridging fault resistance between nodes Vn0 and Vn1. In the first case, both level shifters are functional thus the outputs of the level shifters are VDDH (1.7V). We ran the simulations using different values of bridging fault resistance, from 100Ω to 5MΩ. Selective significant results are presented in Table I as the Single Fault Case. The 'Actual Path Delay' is measured from the time when the input signals reach 50% of VDDL to the time the output signals reach 50% of VDDH. The Path Delay ratio is calculated by taking the ratio between the delay without the bridging fault to the delay when the R_bridge is present.

In the Double Fault Case, one of the level shifters (B) is assumed to be defective. The defective level shifter cannot bring the signal up to VDDH and will give a degraded output (VDDL). The delay ratio in this case is the ratio between these two delays i.e. the 'Actual Path Delay' and delay measured for the defective level shifters but without the bridging fault.The results are shown as the 'Double Fault Case' in Table I.

From Table I we observe that the actual delay increases when the defective input from the level shifter is used as an input. The increase in delay is more significant with smaller values of fault resistance. Similar observations apply to the path delay ratio.

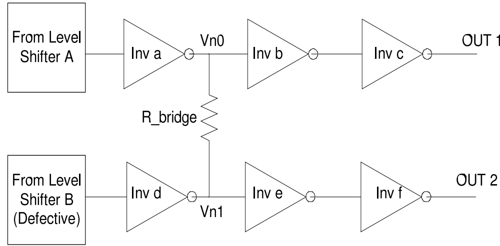

Fig. 1. Circuit model for defective level shifter in presence of bridging fault

TABLE I
PATH DELAY AND PATH DELAY RATIO FOR SINGLE AND DOUBLE FAULTS

R_bridge	Single Fault Case		Double Fault Case	
	Actual Path Delay (s)	Path Delay Ratio	Actual Path Delay (s)	Path Delay Ratio
1M	1.88E-11	1.00	3.37E-11	1.00
25k	1.89E-11	1.01	3.54E-11	1.05
2500	2.09E-11	1.11	9.39E-11	2.79
100	4.59E-11	2.44	52.10E-11	15.50

From the results, we can infer that a defective level shifter will exaggerate the impact of a bridging fault when both faults are present at the same time. These results are useful for two reasons: pattern generation and fault diagnosis. Even though inputs of (1,0) and (0,1) will have higher fault coverage [6], it is important to note that the defective (1,1) input is important for diagnosis reasons. We have demonstrated that this input may detect some of the bridging faults with different voltage domains.

III. PROPAGATION OF FAULT EFFECT IN LEVEL SHIFTERS

In order to include the level shifters in the path of a digital scan chain, it is important to know if the level shifters can propagate the fault effects. To demonstrate this, two types of faults, resistive opens and bridging faults, were used in simulations. The CMLS [4], Figure 2, has been used in all our fault simulations.

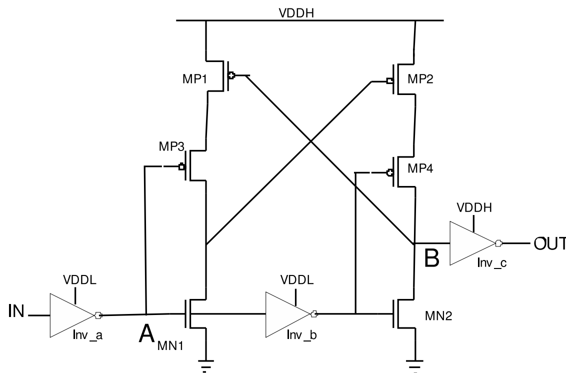

Fig. 2. Contention mitigated level shifter

A. Simulation Setup for Resistive Open Defects

Two blocks of 8 bit ripple carry adders which were linked together were used in the simulations. Resistive open defects were injected and the longest possible path in the circuit was sensitized.

TABLE II
DELAY AND DELAY RATIO FOR CIRCUIT WITHOUT LEVEL SHIFTERS

Resistor Value Ω	Supply Voltage (V)	Actual Delay(s)	Path Delay ratio
0	0.85	3.04E-09	1.00
10000	0.85	3.20E-09	1.06
250000	0.85	1.26E-08	4.14
0	1.70	1.52E-09	1.00
10000	1.70	1.66E-09	1.09
250000	1.70	7.19E-09	4.72

The path delay was measured between the carry in for ADDER block 1 and carry out of ADDER block 2. It is observed that as the value of the resistor increases, the path delay and path delay ratio increase for all values of voltages.

The simulation was repeated by adding a level shifter between the two adders. Table III shows the simulation results. It is evident from Table II and Table III that the level shifter has propagated the fault effect. The path delay ratio for circuit with level shifter resembles the ratio for the circuit without the level shifter.

TABLE III
DELAY AND DELAY RATIO FOR CIRCUIT WITH LEVEL SHIFTERS

Resistor Value Ω	Supply Voltage, V1(V)	Supply Voltage, V2(V)	Actual Delay(s)	Path Delay ratio
0	0.85	1.70	2.36E-09	1.00
10000	0.85	1.70	2.53E-09	1.07
250000	0.85	1.70	1.19E-08	5.04

B. Simulation Setup for Bridging Fault Defects

Firstly, simulations were conducted using the setup without the level shifters as in Figure 3 (a) and later with the level shifters as in Figure 3 (b) to observe if the levels shifters can propagate the fault effects. The bridging faults are injected at the second bit of ADDER1. Four fault locations were randomly chosen from possible fault locations.

The outputs are observed at two locations: at SUM of the second bit and at the third bit of ADDER2. Due to the similarity of the results, only one of the results is presented and discussed in this paper. Table IV and Table V shows the path delay and path delay ratio for both cases: with and without level shifters. Similar observations were made for 3 other fault locations.

These results show that the level shifter can propagate the fault effect. This means that the level shifters can be included in the digital DfT architecture.

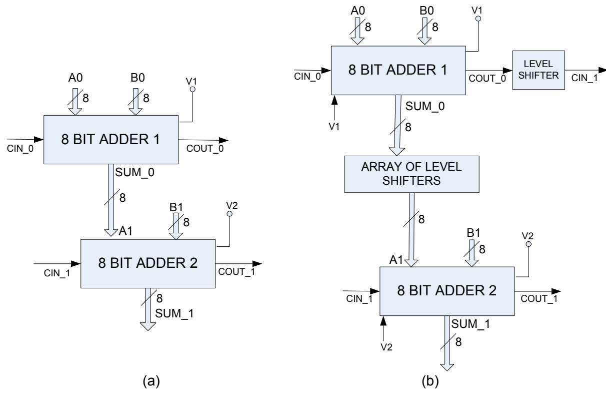

Fig. 3. Simulation setup for bridging fault

TABLE IV
PATH DELAY AND PATH DELAY RATIO FOR CIRCUIT WITHOUT LEVEL SHIFTERS

Resistor Value Ω	Supply Voltage (V)	Actual Delay(s)	Path Delay ratio
500000	0.85	2.32E-10	1.00
5000	0.85	2.46E-10	1.06
500	0.85	4.33E-10	1.87
500000	1.70	1.18E-10	1.00
5000	1.70	1.18E-10	1.00
500	1.70	4.33E-10	3.67

IV. DEFECTS IN LEVEL SHIFTERS

We have simulated a number of possible defects in the circuit and examined at their responses at different supply voltages. The simulations are conducted under two conditions. In the first condition, two voltage domains are used. We introduce the term ACTIVE mode to mean that the level shifter is actively shifting from a low voltage domain to a high voltage domain. ADDER1 uses a low supply voltage and ADDER2 uses a high supply voltage. In the second condition, which we name the PASSIVE mode (no active shifting), all parts of the circuit are operating with the same supply voltage. The two main classes of defects studied in this paper are resistive shorts and resistive opens.

A. Resistive Open

Results from two different fault locations are reported to illustrate the effect of the power supply on path delay ratios for faulty circuits. These locations are at point A and point B in Figure 2. Each fault is injected singly. The setup in Figure 3 (b) was used for all the simulations for resistive opens in both ACTIVE and PASSIVE modes. The faulty level shifter was placed at the first bit of the array of level shifters.

TABLE V
DELAY AND DELAY RATIO FOR CIRCUIT WITH LEVEL SHIFTERS

Resistor Value Ω	Supply Voltage, V1(V)	Supply Voltage, V2(V)	Actual Delay(s)	Path Delay ratio
500000	0.85	1.70	3.20E-10	1.00
5000	0.85	1.70	3.26E-10	1.05
500	0.85	1.70	5.16E-10	1.66

Table VI shows the actual path delay and path delay ratios for different values of resistor. The zero resistance is the fault free value which is then used to calculate the ratio. Comparing this with the results in Table VII shows that as the resistor value is increased, the path delay also increases. This is observed in both PASSIVE and ACTIVE modes for both faults, A and B. It can be observed that not only can the fault be detected in the PASSIVE mode but also it has a better ratio. This implies that the impact of the defect is becomes more visible when the level shifter is in passive mode.

TABLE VI
PATH DELAY AND PATH DELAY RATIO FOR FAULT A AND FAULT B IN ACTIVE MODE, V1=0.85V AND V2=1.7V

Resistor Value Ω	Fault A		Fault B	
	Actual Path Delay (s)	Path Delay Ratio	Actual Path Delay (s)	Path Delay Ratio
0	2.63E-10	1.00	2.63E-10	1.00
25k	3.97E-10	1.51	3.72E-10	1.42
500k	2.05E-09	7.81	2.01E-09	7.64
1M	1.06E-08	40.36	1.08E-08	41.08

TABLE VII
PATH DELAY RATIO FOR FAULT A AND FAULT B IN PASSIVE MODE

V_{dd}	Fault A			Fault B		
	25k	500k	1M	25k	500k	1M
1.70	1.92	11.75	71.52	1.92	13.90	78.26
1.40	1.81	10.68	63.36	1.80	12.20	68.42
1.20	1.71	9.71	56.13	1.70	10.68	59.67
1.00	1.59	8.45	47.04	1.58	8.83	48.89
0.85	1.49	7.24	38.73	1.48	7.28	39.45

It can also be observed that the delay ratio increases with the voltage for a fixed value of resistance. This suggests that the highest operating voltage is prefered to achieve better fault coverage.

B. Resistive Short

Resistive short faults were injected at different points in the level shifters. Five different locations of the defects are shown as R_a, R_b, R_c, R_d and R_e in Figure 4. Rather than reporting the full detailed results of the simulation, we have selected two faults and present their results. These are at locations R_a and R_d.

C. Simulation Results

The simulation results for resistive shorts for both the ACTIVE and PASSIVE modes are tabulated in Table VIII and Table IX, respectively. It can be noted that some of the faults cause speed up. In some cases the speed up is up to 26% as in the case of R= 1.5kΩ, fault R_d, ACTIVE mode. Here, the resistive short causes imbalance in the symmetry of the level shifter circuit and causes the speed up. Even though the speed up will not cause any performance degradation or logical

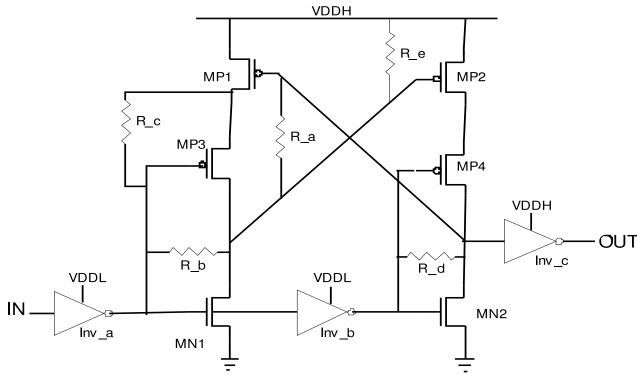

Fig. 4. Defect location for resistive shorts

error, it is important to detect these faults. An undetected fault might cause other performance degradation in a different circuit environment. SF in the table means the result is a logical error and is categorized as a Stuck at Fault. These faults can be detected both by means of delay fault testing as well as stuck-at-fault testing.

TABLE VIII
PATH DELAY AND PATH DELAY RATIO FOR FAULT R_A AND FAULT R_D IN ACTIVE MODE, V1=0.85V AND V2=1.7V

Resistor Value Ω	Fault R_a Actual Path Delay (s)	Fault R_a Path Delay Ratio	Fault R_d Actual Path Delay (s)	Fault R_d Path Delay Ratio
10M	2.63E-10	1.00	2.63E-10	1.00
3000	2.56E-10	0.97	2.10E-10	0.80
1500	2.90E-10	1.11	1.94E-10	0.74
1000	3.94E-10	1.50	-	SF
750	-	SF	-	SF

TABLE IX
PATH DELAY RATIO FOR FAULT R_A AND FAULT R_D IN PASSIVE MODE

	Fault R_a			Fault R_a		
V_{dd}	3K	2k	1500	3K	2k	1500
1.70	0.97	0.96	0.94	0.97	0.96	0.94
1.40	0.97	0.96	0.84	0.97	0.96	0.84
1.20	0.97	0.95	SF	0.97	0.95	SF
1.00	0.97	SF	SF	0.97	SF	SF
0.85	0.97	SF	SF	0.97	SF	SF

These results clearly suggest that a PASSIVE mode test will result in better fault detection. It is also preferable to conduct the test at the lowest possible voltage in order to have the highest fault coverage for the case of resistive short faults. As can be observed, the lowest supply voltage i.e 0.85V in PASSIVE mode will detect resistive shorts up to 2.5kΩ. On the other hand, the highest voltage, 1.7V, in ACTIVE mode can only detect resistive shorts smaller than 1kΩ for Fault D.

From the simulation results for the four different faults, it can be observed that a fault in the level shifters can be detected using a digital fault model, either the stuck-at or delay fault model. Another important observation is that the fault can be detected at a single supply voltage i.e in the PASSIVE mode. The question then arises as to which voltage gives better fault coverage. From Table VII a higher voltage gives a better path delay ratio for resistive open defects. This signifies that there will be a larger variation in the path delay between the fault-free and faulty circuits at higher voltages. For the case of resistive shorts, Table IX shows that the path delay ratio is more pronounced at a lower voltage. However, testing at a lower voltage will increase the test application time [3].

V. CONCLUSION

We have considered testing level shifters in a multi-voltage design. To the best of our knowledge, this is the first study of these issues in relation to multi-voltage systems. Our experiments show how a defect in a level shifter can cause performance degradation in term of timing as well as functional failure. A bridging fault effect will be amplified in the presence of a defective level shifter.

The key findings of this work which relate to the two initial questions are:

- The level shifter can be tested as a digital circuit using conventional Design-For-Test(DFT). This is justified since the defects in level shifters cause digital effects. In addition, level shifters can also propagate digital fault effects such as resistive opens and shorts.
- The level shifters can be tested using a single supply voltage, in the PASSIVE mode.
- To achieve maximum fault detection, the level shifters have to be tested in the PASSIVE mode at two voltage settings: the lowest and highest voltages. Resistive open faults have a better fault ratio at the highest voltage but resistive shorts have a better fault ratio at the lower voltage.

Our intention is now to apply this work to systems with Dynamic Voltage Scaling in order to derive suitable testing strategies.

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