Procedural Analog Design (PAD) Tool

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Abstract

*This paper presents a new **P**rocedural **A**nalog **D**esign tool called **PAD**. It is a chart-based design environment dedicated to the design of analog circuits aiming to optimise design and quality by finding good tradeoffs.*

This interactive tool allows step-by-step design of analog cells by using guidelines for each analog topology. At each step, the user modifies interactively one subset of design parameters and observes the effect on other circuit parameters. At the end, an optimised design is ready for simulation (verification and fine-tuning). Furthermore, PAD provides a layout generator for matched substructures such as current mirror, cascode stage, differential pair, etc.

The analog basic structures calculator embedded in PAD uses the complete set of equations of the EKV MOS model, which links the equations for weak and strong inversion in a continuous way[1,2].

The present version of PAD covers the procedural design of transconductance amplifiers (OTAs) and different operational amplifiers topologies.

1. Introduction

Many CAD tools and environments have been proposed to facilitate the design task and increase circuit quality. At system-level, the design flow for mixed-mode circuits uses different ways and methodologies to design and layout analog and digital parts (Figure 1).

For digital circuitry, the design procedure can be strongly automated. It consists of: circuit specification, behavioral modeling, circuit synthesis, layout generation, layout extraction and post layout simulation.

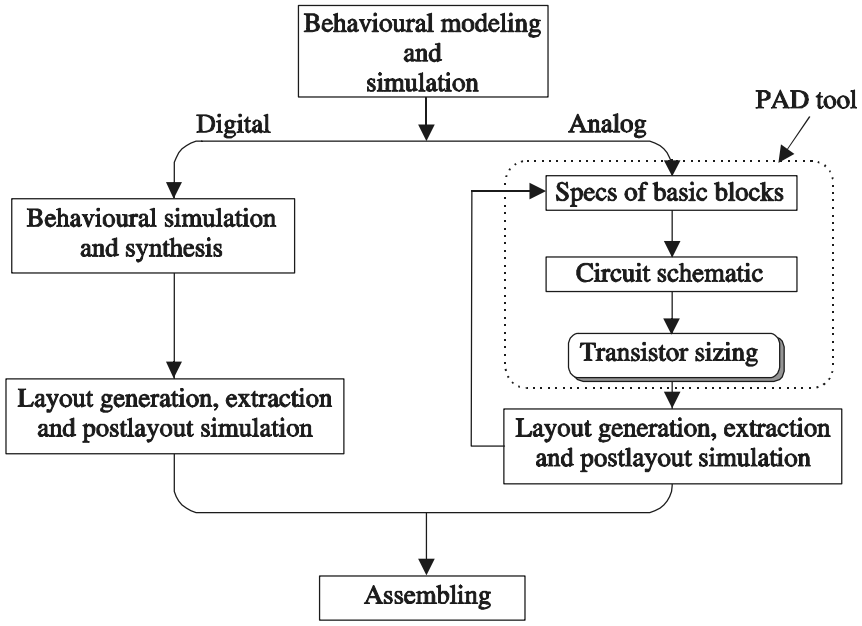

Figure 1. Top down system design approach

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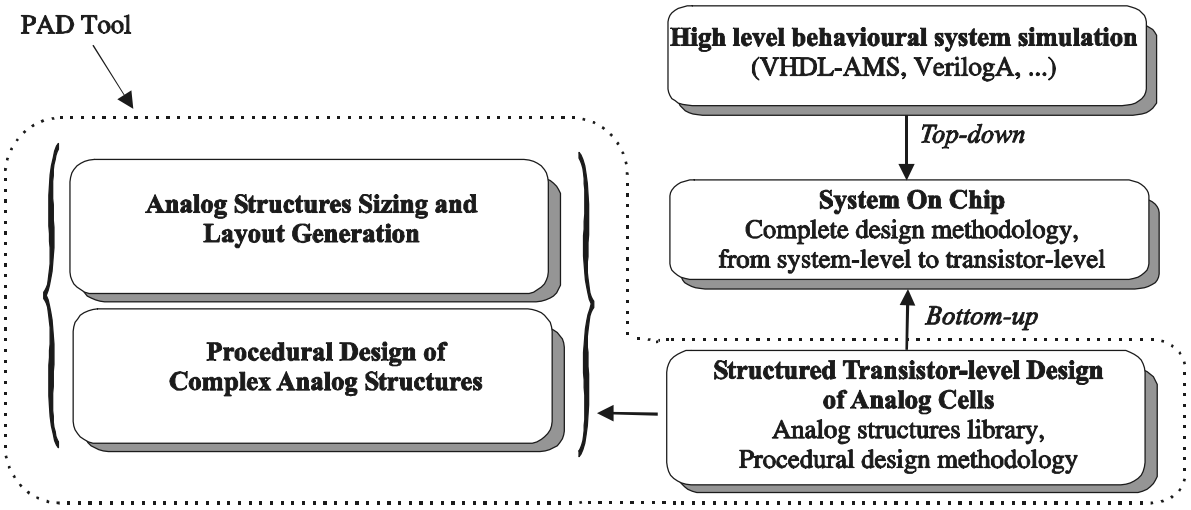

Figure 2. Mixed-mode design flow

This design flow is capable today to automate digital functionalities from behavioral modeling to physical implementation without any transistor-level manipulation, facilitating therefore cells retargeting and technologies migration.

However, for analog functions, the design method depends strongly of the type of the circuit that has to be designed and needs a lot of knowledge at transistor level.

CAD tools for analog design available on the market today cannot provide circuit synthesis from the behavioral description. The problem of topology selection and circuit synthesis leads to transistor-level sizing. This makes the analog design procedure very complicated and automation without user optimisation can be very restrictive. Therefore, retargeting and reuse of circuit topologies is not always possible and needs designer's intervention.

In the recent years many behavioral simulator tools were proposed. They allow designers to simulate their systems at high level. Some of them (VHDL-AMS, VerilogA etc.) use a Spice-like netlist to simulate analog parts of mixed-mode circuits achieving, therefore, behavioral and transistor level simulation.

The proposed PAD tool is dedicated to structured transistor-level design of analog cells. The chart-oriented design tool is very suitable for the design of analog circuits by optimizing design choices and by reducing efforts in determining trade-offs. The best way to find an optimal solution is to combine both approaches: procedural analog design – transistor level simulation and behavioral simulation (Figure 2). The two main purposes of the PAD tool are to reduce expert analog designer's development time and help to hand on analog knowledge toward system level designers. It also facilitates migration of analog libraries from one technology to another.

2. Basic analog structures sizing

The PAD tool presents a new interactive knowledge-based design methodology for analog structures sizing and layout generation. It assists the user by presenting him the necessary theoretical knowledge and tips from an experienced designer. Furthermore, its interactive interface allows instantaneous visualisation of the design tradeoffs. A transistor level calculator is capable of exploring complex relations and displays the results on charts, which the user can interact with. In this way, the PAD tool shows all dependencies and characteristics of analog structures at one glance and allows the designer to discover tradeoffs and to optimise circuits efficiently. For fine-tuning, the simulator can be used interactively with PAD, with a minimal number of simulation runs.

The implemented transistor level calculator uses the complete set of equations based of the EKV MOS model [1,2], which links the equations for weak and strong inversion in a continuous way. The EKV model is very suitable because it enables to find solutions for different input parameter sets without using complex numerical methods. Large number of transistor parameters, which are important for analog design, can be extracted from the model, such as: inversion factor, saturation voltage, Spice-like threshold voltage, Early voltage, small signal parameters, parasitic capacitances, g_m/I_D ratio, transconductance efficiency factor.

The charts enable the transcription of this set of mathematical relations into an appropriate interactive graphical representation. The user-friendly graphic interface has the same appearance for each block. The designer can change different parameters and observe

simultaneously the behavior of the other parameters. In this way, he gets an intuitive understanding of the device behavior.

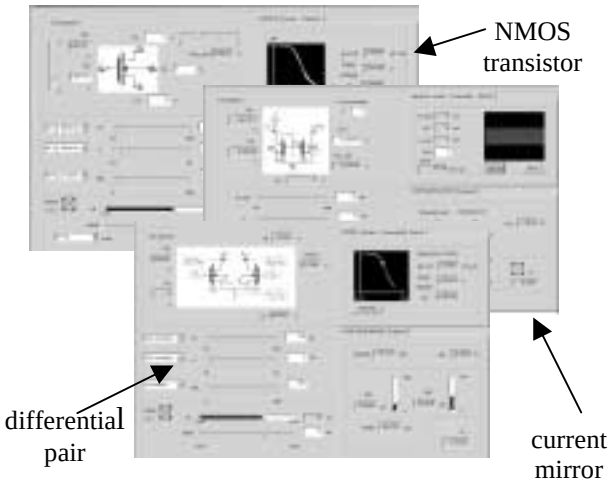

Figure 3. Basic analog structures sizing

An analog structures library is embedded in PAD, including basic analog structures such as: current mirror, differential pair, cascode stage, cascode current mirrors, etc. This tool also allows the analysis of single transistors (NMOS, PMOS) as basic analog structure. For each structure a set of general parameters (small signal model, DC biasing values, parasitic capacitances, speed, etc.) is displayed. Some specific parameters are also shown (maximum DC offset for diff. pair, current mismatch for current mirror, etc). This enables to analyse basic structures behaviour in the environment of a given circuit, and observe parameters that are important for design trade-offs.

The proposed design procedure includes the choice of the g_m/I_D ratio as a measure of the translation of current into transconductance (g_m efficiency and consumption efficiency) [3,4]. At the same time, it gives an indication of the device operating region (strong, moderate or weak).

The basic analog structure sizing consists in setting priority targets (gain, noise, speed). After the bias current is set and the g_m/I_D ratio is chosen according to circuit specifications, the only variables to change are: transistor width W and transistor length L. Simultaneously, the changes of all other parameters can be observed. This methodology can be used for sizing, as well as for optimisation and resizing of circuit blocks.

After successful sizing of the given analog structures, the tool helps the designer to automatically generate matched layout (based on existing layout rules) in CIF format.

Examples of chart-oriented basic analog structures sizing are shown in Figure 3.

3. Example of procedural design of folded cascode OTA using PAD

The procedural design of complex analog structures is also implemented. The current PAD tool version enables systematic design of operational transconductance amplifiers (OTAs) and different operational amplifiers structures. Each of these structures is partitioned into basic analog blocks and the procedural design methodology is applied.

The procedural design flow is illustrated here on the example of a folded cascode OTA. Snapshots of the user interface for each step in the PAD design flow are shown in Figure 4.

The well-known scheme frequently used by analog designers is shown in Figure 5. The usual procedure performed by analog designers is to divide the circuit into basic analog blocks and to derive a set of equations that describe circuit behavior. The folded cascode OTA can be divided into the following basic analog structures (Figure 5):

1. bias 1 – p current mirror
2. bias 2 – n current mirror
3. folded cascode pair
4. cascode current mirror
5. bias 3 – bias for cascode current mirror
6. bias 4 – bias for cascode pair

Circuit level design equations are given in Table I. Using this equation set and running simulation cycles, the designer tries to discover trade-offs and to achieve given circuit specifications.

The procedural analog design flow implemented in PAD for the design of complex analog structures consists of: circuit partitioning into basic analog structures, chart-based basic analog structures sizing and circuit level design. For the folded cascode OTA structure, the PAD design sequence is as follows:

- initialisation
- circuit partitioning
- determination of the circuit currents Io, I1, I2
- sizing of the basic analog structures
- frequency analysis, circuit summary, noise and offset analysis
- simulation runs for fine tuning

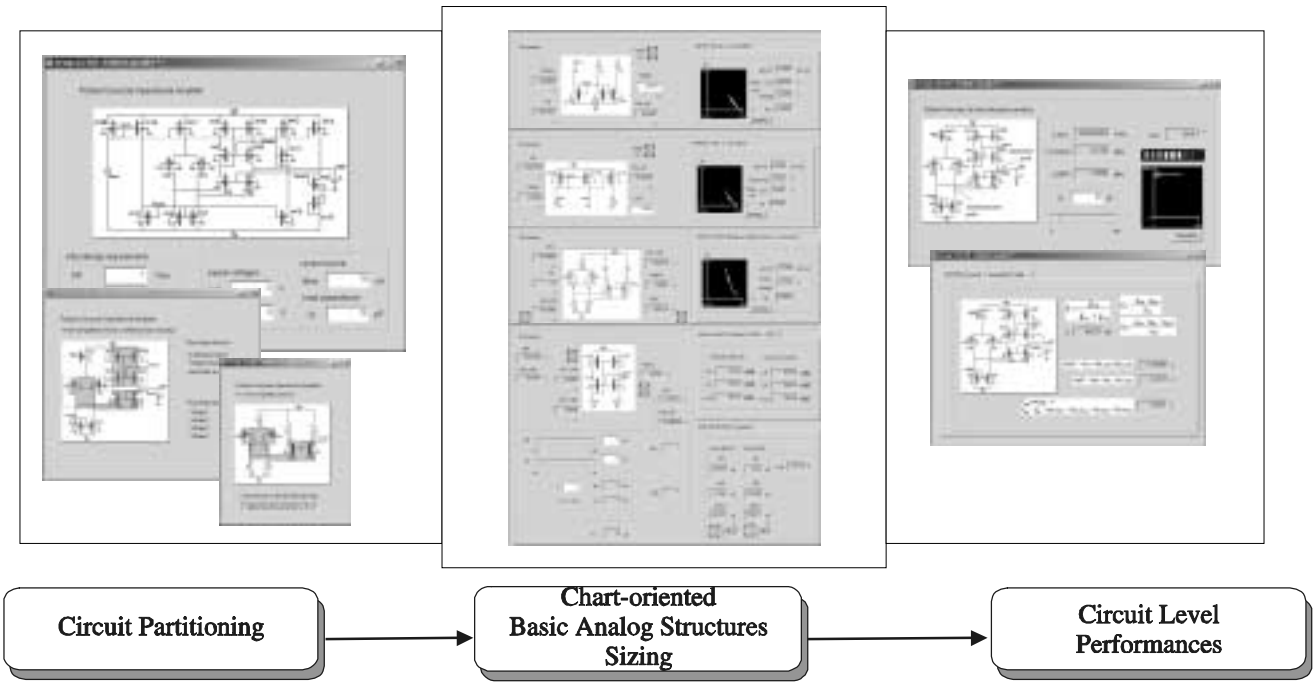

Figure 4. PAD design flow

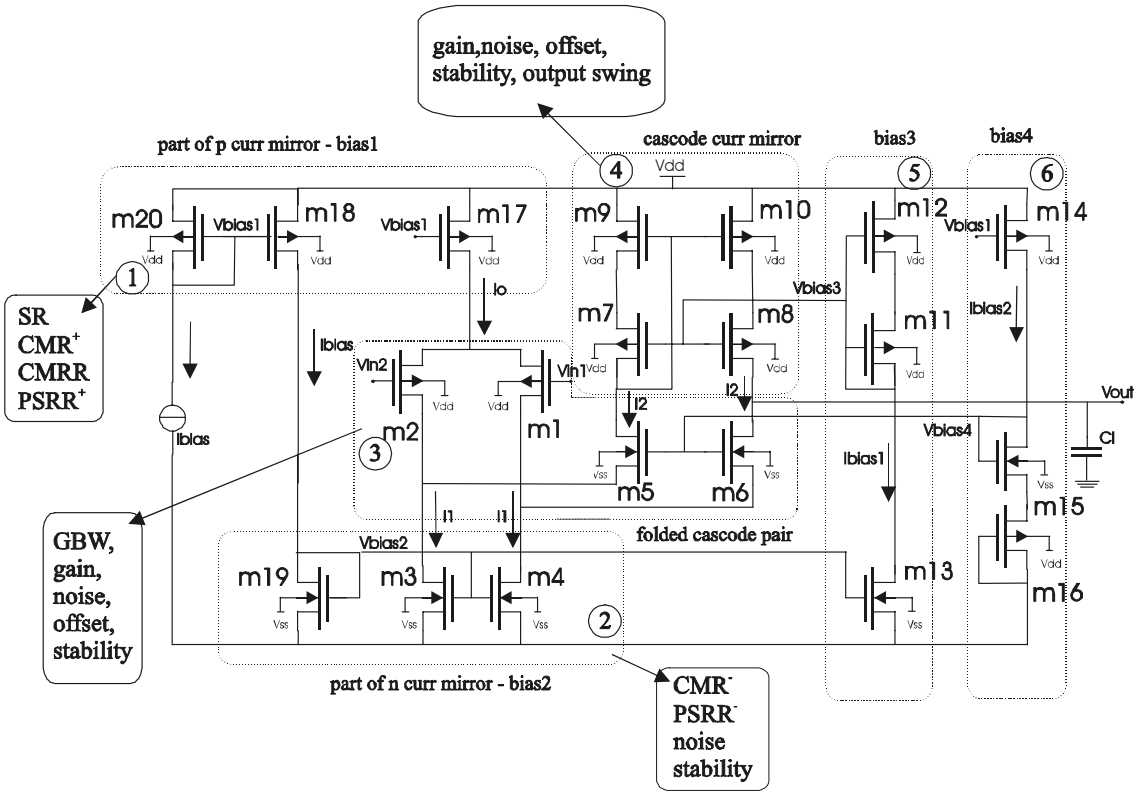

Figure 5. Folded cascode OTA divided into basic analog structures

Table 1. Equations for folded cascode OTA design

slew rate	$SR = \frac{Io}{C_L}$
gain bandwidth frequency	$f\_GBW = \frac{g_{m1}}{2\pi C_L}$
power dissipation	$PowDisip = (V_{dd} - V_{ss}) \cdot (2 \cdot I_1 + 2 \cdot I_{bias} + I_{bias1} + I_{bias2})$
gain	$A = \frac{g_{m1}}{g_{ox} + g_{oy}}, g_{ox} = \frac{g_{ds8} \cdot g_{ds10}}{g_{m8}}, g_{oy} = \frac{g_{ds6} \cdot (g_{ds1} + g_{ds4})}{g_{m6}}$
positive/negative CMR	$CMR+ = V_{dd} - \lvert V_{ds\_sat17} \rvert - \lvert V_{th1} \rvert$ $CMR- = V_{ss} + V_{ds\_sat4} + \lvert V_{ds\_sat1} \rvert - \lvert V_{th1} \rvert$
output swing	$V_{out\_swing} =$ $V_{dd} - V_{ss} - (\lvert V_{ds\_sat8} \rvert + \lvert V_{ds\_sat10} \rvert + V_{ds\_sat6} + V_{ds\_sat4})$
equivalent noise	$v\_eq^2 = v\_eq_1^2 + v\_eq_2^2$ $+ \left(\frac{g_{m4}}{g_{m1}}\right)^2 (v\_eq_3^2 + v\_eq_4^2) + \left(\frac{g_{m9}}{g_{m1}}\right)^2 (v\_eq_9^2 + v\_eq_{10}^2)$
input offset	$V_{off}^2 = (\sigma(\delta V_{G1}))^2 + \left(\frac{g_{m4}}{g_{m1}}\right)^2 (\sigma(\delta V_{G4}))^2 + \left(\frac{g_{m9}}{g_{m1}}\right)^2 (\sigma(\delta V_{G9}))^2$ $(\sigma(\delta V_G))^2 = \sigma_T^2 + \left(\frac{I_D}{g_m}\right)^2 \cdot \sigma_\beta^2$ $\sigma_T = \frac{A_{Vt}}{\sqrt{WL}}, \sigma_\beta = \frac{A_\beta}{\sqrt{WL}}$
pole estimations and phase margin	$f\_p_1 = \frac{g_{ox} + g_{oy}}{C_L}, f\_p_2 = \frac{g_{m6}}{C_{g6} + C_{d4} + C_{d1}}$ $PM = 180^\circ - arctg\left(\frac{f\_GBW}{f\_p_1}\right) - arctg\left(\frac{f\_GBW}{f\_p_2}\right)$

Initialisation - The user is asked to enter:

- EKV technology parameters
- initial design requirements: slew rate SR, gain bandwidth f_GBW
- the bias current I_{bias} and the power supply voltages V_{ss}, V_{dd}, the load capacitance C_L

Circuit partitioning – The folded cascode OTA is divided into the same 6 basic analog structures shown in Figure 5. The implemented set of equations in PAD is the same as in Table I.

Basic analog structures sizing - From the initial design requirements two values are proposed:

$Io\_calc = SR \cdot C_L$

$g_{m1}\_calc = 2\pi f\_GBW \cdot C_L$

From then on, the designer follows the given design procedure for sizing every analog block, as described above. For each block the designer can modify the parameters and observe the impact of his decisions on circuit performances. The most important point is to determine the circuit currents according to the imposed SR value, as well as the g_m for every transistor according to circuit performances. For each basic analog structure, Figure 5 shows a list of dependent circuit parameters.

Circuit level design – During the sizing of each block, circuit performance parameters can be checked. After having designed all building blocks, circuit-level behavior is summarized and the interface to a simulator is proposed.

This design procedure can be repeated several times in interaction with the simulator. The number of simulation runs is reduced to minimum. Transistor sizing and circuit optimisation can be achieved at the same time.

4. Practical example of Miller Op Amp design

Analog library is designed and integrated in 0.5 um MIETEC technology using predifused sea of gate layout structure. Figure 6. shows the die photo of Miller OpAmp cell.

The circuit is designed using PAD in interaction with the simulator. In Table 2 the results of PAD calculation and PSpice simulation, with the load capacitance of 1pF (analog cell library for the internal use only), are

compared. The distribution of measurement results is in good agreement with PAD and simulation results.

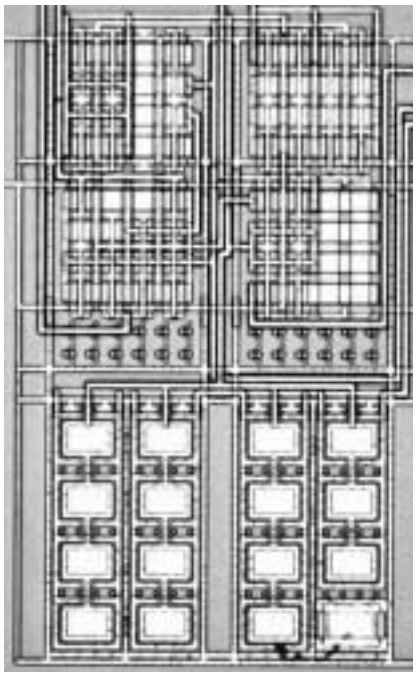

Figure 6. Circuit micrograph

Table 2. PAD calculation and simulation results comparison

	PAD	PSpice
A (dB)	117	106
SR (V/us)	3.3	2.6
f_GBW (MHz)	2.2	2
PM (°)	63	68

5. Conclusion

This paper has presented a new chart-based Procedural Analog Design (PAD) tool and a new knowledge based analog design methodology. The PAD tool allows to encapsulate design knowledge and experience into a CAD tool and to hand them on to other designers.

The interactive PAD tool enables design and re-design of a wide range of circuits. Present version covers the most commonly used analog circuits. For the other circuits, basic analog structures library can be used for separate blocks sizing. The simulator is then used interactively for fine tuning, with minimal number of simulation runs. In this way, a great improvement of analog design quality can be achieved.

6. References

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