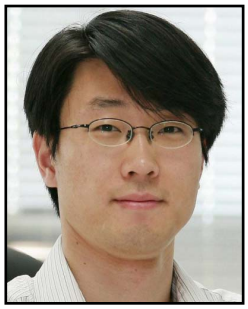
Session 15 Overview: *Data-Converter Techniques*

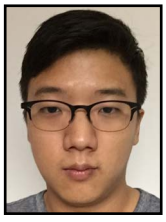
DATA CONVERTERS SUBCOMMITTEE



Session Chair: *Seung-Tak Ryu, KAIST, Daejeon, South Korea*

Session Co-Chair: *Matt Straayer, Maxim Integrated, Chelmsford, MA*

The demands for low power and increased bandwidth continue to be a primary motivation for ADCs. However, the system requirements also present demands on the ADC that can drive design choices at the architectural level. This session demonstrates multiple design techniques for realizing high-performance data converters targeted at a variety of applications and process technologies. Papers in this session include high-performance continuous-time delta-sigma ADCs, a PVT-insensitive TDC implemented in 14nm FinFET technology, and new buffering techniques for both reference voltages and input signals. These papers represent multiple advances in capability for low-power, wide-bandwidth, and high-performance data converters.



15.1 An 85dB-DR 74.6dB-SNDR 50MHz-BW CT MASH ΔΣ Modulator in 28nm CMOS **1:30 PM**
D-Y. Yoon, Massachusetts Institute of Technology, Cambridge, MA

In Paper 15.1, MIT and MediaTek present a ΔΣ modulator in 28nm LP CMOS that utilizes a 3-1 continuous-time Sturdy-MASH architecture to achieve aggressive noise shaping with a 50MHz bandwidth. It is clocked at 1.8GHz and achieves 85.2dB SFDR and 74.6dB SNDR while consuming 78mW.

15.2 A 4.5mW CT Self-Coupled ΔΣ Modulator with 2.2MHz BW and 90.4dB SNDR Using Residual ELD Compensation **2:00 PM**
C-Y. Ho, MediaTek, Hsinchu, Taiwan

In Paper 15.2, MediaTek presents a continuous-time self-coupling (CTSC) ΔΣ modulator with residual ELD compensation and DAC linearity enhancement techniques. The ADC achieves an SNDR of 90.4dB with a 2.2MHz bandwidth. It is implemented in 55nm CMOS and consumes 4.5mW.

15.3 A 115dB-DR Audio DAC with –61dBFS Out-of-Band Noise **2:30 PM**
H. Westerveld, University of Twente, Enschede, The Netherlands

In Paper 15.3, University of Twente, Delectronics, and Teledyne DALSA present a ΔΣ audio DAC with a 2-path approach that reduces out-of-band noise to below -60dBFS, allowing for a very small area and power-efficient implementation. Fabricated in 0.08mm^2 of 0.18µm CMOS, the dynamic range and THD+N are measured at 115dB (A-Weighted) and -103dB, respectively.

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15.4 A 0.8V 10b 80kS/s SAR ADC with Duty-Cycled Reference Generation **2:45 PM**

M. Liu, Eindhoven University of Technology, Eindhoven, The Netherlands

In Paper 15.4, TU Eindhoven presents a 10b 80kS/s SAR ADC in 65nm CMOS with a 0.62V reference-voltage generator (RVG). To save power, the RVG is operated at 10% duty cycle, and a bi-directional dynamic comparator is employed. The ADC achieves 56.6dB SNDR and 65.0dB SFDR at Nyquist with an efficiency of 2.4fJ/conversion-step.

15.5 A 0.6V 1.17ps PVT-Tolerant and Synthesizable Time-to-Digital Converter Using Stochastic Phase Interpolation with 16× Spatial Redundancy in 14nm FinFET Technology **3:15 PM**

S-J. Kim, Samsung Electronics, Hwaseong, Korea

In Paper 15.5, Samsung presents a low-power and PVT-variation-tolerant TDC featuring stochastic phase interpolation and 16× spatial redundancy. The converter architecture leverages 14nm FinFET CMOS technology to achieve high linearity and 1ps resolution without any calibration.

15.6 A 12b 250MS/s Pipelined ADC with Virtual Ground Reference Buffers **3:45 PM**

H. H. Boo, Massachusetts Institute of Technology, Cambridge, MA

In Paper 15.6, MIT presents a virtual ground reference buffer approach for switched-capacitor circuits that significantly relaxes key op-amp specifications including unity-gain bandwidth, noise, and open-loop gain. The technique is demonstrated with a 12b 250Ms/s pipeline ADC in 65nm CMOS that achieves 67dB SNDR with 49.7mW power consumption.

15.7 A 14b 35MS/s SAR ADC Achieving 75dB SNDR and 99dB SFDR with Loop-Embedded Input Buffer in 40nm CMOS **4:15 PM**

M. Krämer, Stanford University, Stanford, CA

In Paper 15.7, Stanford University and NXP Semiconductors present a 14b 35MS/s SAR ADC in 40nm CMOS with a loop-embedded input buffer that consumes only 23% of the total ADC power. The buffer uses a source follower (SF) topology whose nonlinearities are cancelled by the SAR algorithm, achieving 99dB SFDR despite the small amount of invested power.

15.8 A 90dB-SFDR 14b 500MS/s BiCMOS Switched-Current Pipelined ADC **4:45 PM**

M. El-Chammas, Texas Instruments, Dallas, TX

In Paper 15.8, Texas Instruments presents a 14b 500MS/s pipelined ADC in 0.18µm BiCMOS SiGe targeted for wireless infrastructure applications. Track-and-hold enhancements and extended amplifier settling time are used to achieve over 90dB SFDR at low frequency and over 80dB up to 500MHz inputs.