Published in final edited form as:
IEEE Trans Biomed Eng. 2013 May ; 60(5): 1414–1421. doi:10.1109/TBME.2012.2237172.

Simplified Design Equations for Class-E Neural Prosthesis Transmitters

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Abstract

Extreme miniaturization of implantable electronic devices is recognized as essential for the next generation of neural prostheses, owing to the need for minimizing the damage and disruption of the surrounding neural tissue. Transcutaneous power and data transmission via a magnetic link remains the most effective means of powering and controlling implanted neural prostheses. Reduction in the size of the coil, within the neural prosthesis, demands the generation of a high-intensity radio frequency magnetic field from the extracoporeal transmitter. The Class-E power amplifier circuit topology has been recognized as a highly effective means of producing large radio frequency currents within the transmitter coil. Unfortunately, design of a Class-E circuit is most often fraught by the need to solve a complex set of equations so as to implement both the zero-voltage-switching and zero-voltage-derivative-switching conditions that are required for efficient operation. This paper presents simple explicit design equations for designing the Class-E circuit topology. Numerical design examples are presented to illustrate the design procedure.

Keywords

Class-E; inductive coupling; neural prosthesis implant; transmitter

I. Introduction

As fully implantable magnetically powered neural prosthesis devices become smaller, the need for generating an intense magnetic field in the extracorporeal transmitter coil becomes a requirement due to the low-valued coefficient of coupling. Since for miniature devices the secondary (implanted) coil is often millimeter or submillimeter sized, the inductive coupling coefficient k is in the range of $10^{-5} < k < 10^{-3}$ [1]. Therefore, the only viable design approach for powering the implantable device becomes that of creating a high-intensity magnetic field at radio frequencies. Since most proposed systems would use battery power for the extracorporeal transmitter, the design challenge is that of producing the large current

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in the primary coil in order to power the implanted device, while minimizing the power drawn from the transmitter battery.

One transmitter topology that is ideally suited for generating large transmitter coil currents, at radio frequencies, is the Class-E power amplifier. The Class-E power amplifier was introduced by Sokal and Sokal in 1975 [2] and fully analyzed by Raab in 1977 [3]. The technology was investigated for use in the biomedical engineering field in the early 1990s. Zierhofer and Hochmair [4] made a self-oscillating Class-E circuit that changes its oscillation frequency in the primary coil in order to maintain the coupled voltage in the secondary coil insensitive to the distance variation between the primary and secondary coils. Troyk and Schwan [5]–[7] invented a current-mode feedback circuit that controls the transistor switch in the Class-E circuit to turn-on at the correct time, within the oscillator cycle, so that the circuit is always maintained in near-Class-E high-efficiency mode, despite changes in the tuning of the multifrequency resonant network. The Class-E circuit topology has been used for inductively coupled transcutaneous transmission of power and data in various implantable neuroprosthetic devices, including cochlear implants [8], visual prosthesis stimulators [9], microstimulators [10], and neural recording devices such as the implantable myoelectric sensor (IMES) [11].

As shown in the circuit diagram (see Fig. 1), the classical Class-E circuit topology consists of a series *LC* tuned load network (C_{series}, L, and R), a shunt capacitor C_{shunt}, a dc current I_{DC} that is usually supplied by an RF choke inductor in series with the power supply V_{DC}, and an active switching transistor FET. The synchronous transistor switching sustains an oscillating coil current $i_p(t)$ by replenishing the energy loss in the resistive load R, during each cycle of operation. To implement the Class-E conditions, the transistor voltage and current waveforms are ideally timed so that at the moment of switching, the transistor voltage is zero and has zero slope; therefore, the power loss within the transistor is theoretically zero, i.e., the Class-E circuit has 100% power efficiency. In practice, the transistor voltage does not remain at zero during the conduction portion of the cycle due to the finite on-resistance of the transistor, and although the circuit can operate with extremely low loss, 100% efficiency is not achievable.

To maintain the high-efficiency operation, the transistor in the circuit has to meet both zero-voltage switching (ZVS) and zero-voltage-derivative switching (ZVDS) conditions. In theory, the circuit component values can be calculated using a set of cumbersome analytical equations. Most often, in practice, Class-E power amplifiers are typically manually tuned because of the high sensitivity to slight deviations in the operating point and circuit component values from the ideal design values. To alleviate this often intractable tuning problem, Troyk and Schwan devised the current-mode closed-loop Class-E circuit [5]–[7]. For transmitter coils that are characterized by a very high quality factor, i.e., low loss, this approach uses a current-sense transformer to measure the inductor L current and maintain the Class-E conditions. This method compensates well for inevitable changes in the parasitics or shape of the transmitter coil that can often result in rapid destruction of the transistor switch due to excessive power dissipation as the circuit moves off of the precise Class-E frequency. Using the current-mode closed-loop control, typically, a 10–20% switch

duty cycle is used, limiting the power dissipated in the transistor switch and minimizing the battery power supply current.

While effective at maintaining near Class-E operation, the feedback loop only implements the ZVDS condition. To operate in a high-efficiency mode, the circuit also has to satisfy the ZVS condition, such that during each cycle when the transistor switch begins conduction, there is zero charge left on the shunt capacitor to avoid excessive heat loss. To configure a particular Class-E circuit design for the ZVS condition, the complicated circuit equations must be solved; alternatively, a trial-and-error approach is employed. It is the purpose of this paper to present design equations for easily calculating the Class-E circuit components needed for high-efficiency mode at any duty cycle. Our approach, commonly called “design oriented analysis” (D-OA, a methodology advocated by Middlebrook [12]), is different from most of the Class-E power amplifier analyses in the literature. In those analyses, the circuit component values are entangled with the design requirements (e.g., input/output power, operating frequency, etc.) in complicated implicit equations that can only be solved numerically. Using D-OA, preferred circuit component values are specified on the left side and design requirements on the right side of the equations.

The distinction of using D-OA is mainly due to the different nature of analysis versus design. For instance, in Raab’s Class-E circuit analysis [3], ZVS and ZVDS conditions of the collector voltage $v(\theta)$ were applied as boundary conditions after the voltage formula was subject to the Fourier transform. This is a typical approach for an analysis that starts from a general case and reduces to the more specific one by applying the boundary conditions one by one. But it results in many complicated implicit equations of $v(\theta)$, in which circuit component values are almost impossible to analytically determine. To give an illustrative example, to determine the relationship between the duty cycle y[1] and the current ratio g,[2] one has to eliminate the phase angle ϕ from (3.2), $\cos(\phi) = y/(g \sin y)$, and (3.8), $\tan(\phi) = \cot y - 1/y$, in Raab’s paper and solve the implicit equation

$$\frac{\sqrt{1-\left(\frac{y}{g\ sin(y)}\right)^2}}{\frac{y}{g\ sin(y)}} = \pm\left(cot\,(y) - \frac{1}{y}\right).$$

In Section II, we arrive at a mathematically equivalent but simpler equation for this relationship. In addition, we also derive explicit equations for the other circuit component values. The D-OA technique used to reach those simplified formulas is implemented by making reasonable initial assumptions and by including known/boundary conditions early during the derivation.

II. Design Equations

Typically, the analysis of the Class-E circuit (see Fig. 1) starts from the output coil current $i_p(t)$. By using the high-Q approximation of the series LC_{series} branch [5], we can assume

[1]We use Raab’s notation temporarily. Note that it is different from our definition later.
[2]$g = I_p/I_{DC}$

$i_p(t)$ to be sinusoidal and define it as $i_p(t) = I_p \sin(\omega t + \phi)$, where ω is the operating frequency of the Class-E circuit, I_p is the amplitude of the coil current, and ϕ is the phase angle. This phase angle is an unknown variable that depends on the timing of the transistor switch. The next step is to derive the expression for the transistor voltage $v_s(t)$. In this case, $v_s(t)$ is also the voltage at the node of the capacitor C_{shunt}, which is charged by the current $i_s(t)$ when the transistor is not conducting. During that time period, $i_s(t)$ is the sum of the dc current I_{DC} from the power supply and the coil current $i_p(t)$. On arriving at an expression for $v_s(t)$, one can apply the boundary conditions ZVS and ZVDS to obtain equations for the unknowns in the expression. The frequency analysis of $v_s(t)$ via Fourier transform at the fundamental frequency ω can relate the reactance of the circuit to L and C_{series}. Finally, the input and output power balance equation relates the power supply parameters V_{DC} and I_{DC} with the output parameters I_p and R. Given these analytical equations combined with a sufficient number of inputs values, the unknown variables can usually be solved numerically.

However, our D-OA approach is almost the reverse of the conventional procedures described above. We begin the derivation from the energy balance equation.

The high-Q approximation not only assumes $i_p(t)$ as being sinusoidal, which facilitates the Fourier analysis later, but it also implies that the power loss of the sinusoidal current $i_p(t)$ in the resistor load R can be simply expressed as

$$P_{out} = \frac{1}{2} R \cdot I_p^2. \quad (1)$$

Assuming that this is the only power loss in the circuit (i.e., no loss on the transistor or by harmonic currents), and the circuit is running at 100% power efficiency, the input and output power should balance out:

$$P_{out} = \frac{1}{2} R \cdot I_p^2 = P_{in} = I_{DC} \cdot V_{DC}. \quad (2)$$

For the closed-loop Class-E circuit that drives a low-loss coil, the high-Q approximation is reasonable because R in the circuit is mainly caused by the small-valued coil wire resistance, and the quality factor Q_L can be in the range of 100–300.

In Section III, (2) is modified to take into account the power loss due to the on-resistance of the transistor.

From (2), we define an intermediate variable: current ratio α as the ratio between I_{DC} and I_p

$$\alpha = \frac{I_{DC}}{I_p} = \frac{I_p \cdot R}{2 V_{DC}}. \quad (3)$$

According to (3), α can be calculated once the power supply voltage V_{DC}, the coil current amplitude I_p, and the coil resistance R are specified. These are usually available at the onset of the design, since the physical configuration, and the resulting electrical requirements of

the transmitter coil, is a frequent starting point for the transmitter design. In most cases, R can be calculated uniquely from the quality factor Q_L in

$$Q_L = \frac{\omega L}{R} \quad (4)$$

where Q_L, L, and the operating frequency ω are given as the basic coil characteristics.

The only two remaining circuit components are C_{shunt} and C_{series}, and determination of these to assure Class-E operation is often the problem which causes researchers to resort to an empirical approach using bench testing or brute force simulation. To obtain the explicit equations for these two variables, we begin by examining the shunt capacitor current $i_s(t)$ directly. From the circuit diagram in Fig. 1, $i_s(t)$ is the sum of the dc current I_{DC} and the coil current $i_p(t)$, and because of the transistor switching, $i_s(t)$ is not a continuous function like $i_p(t)$, but rather a piecewise function. In the following discussion, we align the zero of the x-axis with the turn-on timing of the transistor switching.

To examine the periodic functions in one cycle, we designate $\theta = \omega \cdot t$ as an independent variable, and hence, the capacitor current $i_s(t)$ in a cycle ($0 \le \theta \le 2\pi$) becomes

$$i_s(\theta) = \begin{cases} 0, & \text{if } 0 \le \theta \le 2\pi \cdot d \\ I_{DC} + I_p \sin(\theta + \varphi), & \text{if } 2\pi \cdot d \le \theta \le 2\pi. \end{cases} \quad (5)$$

Here, the duty cycle d represents the percentage of a cycle during which the transistor switch is turned ON (i.e., conducting). Note that some papers define a similar parameter when the transistor is turned OFF (e.g., y in Raab's paper); some also use half of the off-time (e.g., y in Raab's paper); some use time or radian as units, and not percentage. It should also be obvious that I_{DC} is not a dc current from the point of view of the capacitor, since obviously there could be no dc current going through a capacitor. This is because $i_s(\theta)$ is a piecewise function during each cycle. When the transistor is conducting ($0 \le \theta \le 2\pi \cdot d$), it shorts out the capacitor and $i_s(\theta)$ becomes zero. When the transistor is not conducting ($2\pi \cdot d \le \theta \le 2\pi$), I_{DC} effectively acts like a dc offset that raises the sinusoidal current $i_p(\theta + \phi)$. Also note that we specify the coil current flowing into the shunt capacitor as the positive direction. There will be a flip of sign when we are examining the voltage drop on the coil impedance later.

As shown in Fig. 2, the coil current $i_p(\theta)$ is a sinusoidal waveform and $i_p(0) = i_p(2\pi) = 0$. At $\theta = 0$, $i_p(\theta)$ crosses zero and the transistor switch turns ON. After $\theta = 2\pi \cdot d$, the transistor turns OFF and the shunt capacitor current $i_s(\theta)$ appears as a raised and phase-shifted sinusoid. It is essential that $i_s(0) = i_s(2\pi) = 0$ as well, which, as will be evident from (9), satisfies the ZVDS condition precisely. Therefore, the phase angle ϕ in (5) can be derived simply as $-\arcsin(\alpha)$, after introducing the current ratio α:

$$i_s(\theta) = \begin{cases} 0, & \text{if } 0 \le \theta \le 2\pi \cdot d \\ I_p(\alpha + \sin(\theta - \arcsin(\alpha))), & \text{if } 2\pi \cdot d \le \theta \le 2\pi. \end{cases} \quad (6)$$

As illustrative, both the coil current $i_p(\theta)$ and the shunt capacitor current $i_s(\theta)$ are plotted in Fig. 2, where a = 0.1 and d = 0.186.

The only remaining condition required for the Class-E high-efficiency operation is ZVS. It demands that the integral of $i_s(\theta)$ over each cycle, which represents the charge left on the shunt capacitor, is equal to zero. Hence, the current ratio a and the duty cycle d are related in the following equation:

$$\begin{array}{l}\int_{2\pi\cdot d}^{2\pi}\left(\alpha+sin\left(\theta-\arcsin\left(\alpha\right)\right)\right)d\theta=0\\ 2\pi\alpha\left(1-d\right)+sin\left(2\pi\cdot d+\arccos\left(\alpha\right)\right)-\sqrt{1-\alpha^2}=0.\end{array} \quad (7)$$

This is the only implicit equation in our set of design equations. Once the value of a is calculated from the design requirements (3), the variable d can be solved from (7). Modern mathematical software such as *Mathematica*'s **FindRoot** function can easily solve the equation. The duty cycle d as a function of the current ratio a is plotted in Fig. 3. The relation is straightforward enough that a polynomial function (8) can be fitted explicitly using *Mathematica*'s **InterpolatingPolynomial** function. Such an expression can be used in less capable software such as a spreadsheet program:

$$\begin{array}{rl}d\left(\alpha\right)= & 35.1\alpha^{10}+21.19\alpha^9-500.087\alpha^8+1228.98\alpha^7\\ & -1483.26\alpha^6+1060.51\alpha^5-476.62\alpha^4+136.38\alpha^3\\ & -24.55\alpha^2+3.33\alpha+9.79\times10^{-9}.\end{array} \quad (8)$$

The voltage $v_s(\theta)$ on the shunt capacitor can be expressed as the integral of the current $i_s(\theta)$ that charges the shunt capacitor C_{shunt}, after the transistor switch turns OFF. Consequently, $v_s(\theta)$ is also a piecewise and periodic function:

$$\begin{array}{rl}v_s\left(\theta\right) & =\frac{1}{\omega C_{\text{shunt}}}\int_{2\pi\cdot d}^{\theta}i_s\left(x\right)dx\\ & =\begin{cases}0, & \text{if } 0\le\theta\le2\pi\cdot d\\ \frac{I_p}{\omega C_{\text{shunt}}}\left(\alpha\left(\theta-2\pi\cdot d\right)\right. & \\ \left.+sin\left(2\pi\cdot d+\arccos\left(\alpha\right)\right)\right. & \\ \left.-sin\left(\theta+\arccos\left(\alpha\right)\right)\right), & \text{if } 2\pi\cdot d\le\theta\le2\pi.\end{cases}\end{array} \quad (9)$$

As mentioned earlier, the ZVDS condition of $v_s(\theta)$ is equivalent to stating $i_s(0) = 0$, since the capacitor current $i_s(t)$ is the derivative of its voltage $v_s(t)$. Therefore, both ZVDS and ZVD conditions have been satisfied for the derivation of (6) and (7).

The final step is to perform a Fourier analysis on $v_s(\theta)$ from (9). First, the dc component of $v_s(\theta)$ should be equal to the power supply voltage V_{DC}:

$$V_{DC}=\frac{1}{2\pi}\int_{2\pi\cdot d}^{2\pi}v_s\left(\theta\right)d\theta. \quad (10)$$

V_{DC} is most often the desired battery supply and is usually given in the design requirements; therefore, (9) and (10) can be used to solve for C_{shunt}. The result is an explicit formula:

$$C_{\text{shunt}}=\frac{I_p}{2\pi\omega V_{DC}}K \quad (11)$$

for which

$$\begin{aligned} K= \quad & \alpha\left(2\pi^2(1-d)^2+1\right) \\ & -\left(\alpha+2\pi\,(d-1)\,\sqrt{1-\alpha^2}\right)cos\,(2\pi\cdot d) \\ & +\left(2\pi\alpha\,(1-d)+\sqrt{1-\alpha^2}\right)sin\,(2\pi\cdot d)\,. \end{aligned} \quad (12)$$

The parameter *K* ranges from 6.36 to 0 as a function of the current ratio a. In general, the larger the a, the smaller K becomes.

Second, the reactance of the LC_{series} branch at the fundamental frequency ω can be defined as *X*. It can be expressed by the Fourier transform of the shunt capacitor voltage $v_s(\theta)$:

$$-I_pX=\frac{1}{\pi}\int_{2\pi\cdot d}^{2\pi}v_s\,(\phi)\,cos\,(\phi-\arcsin\,(\alpha))\,d\phi \quad (13)$$

for which:

$$X=\omega L-\frac{1}{\omega C_{\text{series}}}. \quad (14)$$

The negative sign in front of I_p is due to the direction of coil current marked in Fig. 1. We can insert (14) into (13) and solve for C_{series}:

$$C_{\text{series}}=\frac{4\pi C_{\text{shunt}}}{H+4\pi\omega^2LC_{\text{shunt}}} \quad (15)$$

for which

$$\begin{aligned} H= \quad & 6\sqrt{1-\alpha^2}\alpha+4\pi\left(2\alpha^2+1\right)(d-1) \\ & +2\alpha\left(\sqrt{1-\alpha^2}\,(cos\,(4\pi\cdot d)-4\,cos\,(2\pi\cdot d))\right. \\ & \left.+\alpha\,(sin\,(4\pi\cdot d)-4\,sin\,(2\pi\cdot d))\right)-sin\,(4\pi\cdot d)\,. \end{aligned} \quad (16)$$

The parameter *H* is also a function of a. It ranges from −12.6 to 0, as a goes from 0 to 1.

To summarize the simplified design procedure, given a design requirement set {dc power supply V_{DC}, coil current amplitude I_p, coil parameters (L, Q_L), and the Class-E operating frequency ω}, the current ratio a can be calculated from (3) and (4). Then, the duty cycle *d* can be solved from (7), using the plot of Fig. 3, or by direct calculation using (8). Finally, the capacitors C_{shunt} and C_{series} can be calculated with (11) and (15) directly.

III. Transistor Power Loss

According to the circuit diagram (see Fig. 1), the transistor conducts the current $i_s(\theta)$ during the time period ($0 \le \theta \le 2\pi \cdot d$) after it turns ON during each cycle. Assuming that the transistor has a constant on-resistance R_{on}, its power loss can be calculated as

$$\begin{aligned} P_t = & \frac{1}{2\pi}\int_0^{2\pi\cdot d} i_s(\theta)^2 R_{on} d\theta \\ = & \frac{R_{on}\cdot I_p^2}{8\pi}\left(6\alpha\sqrt{1-\alpha^2}+4\pi\cdot d\left(1+\alpha^2\right)\right. \\ & -8\alpha\, sin\left(2\pi\cdot d+\arccos\left(\alpha\right)\right) \\ & \left.+sin\left(4\pi\cdot d+2\arccos\left(\alpha\right)\right)\right). \end{aligned} \quad (17)$$

Therefore, an improved energy balance equation to replace (2) would be

$$P_{out}=\frac{1}{2}R\cdot I_p^2+P_t=P_{in}=I_{DC}\cdot V_{DC}. \quad (18)$$

Once we collect the terms involving α and d in (17) into an intermediate function $g(\alpha, d)$, we can rearrange (18) to

$$\frac{1}{2}R+R_{on}\cdot g\left(\alpha,d\right)=\frac{V_{DC}}{I_p}\cdot\alpha \quad (19)$$

for which

$$\begin{aligned} g\left(\alpha,d\right) = & \frac{1}{8\pi}\left(6\alpha\sqrt{1-\alpha^2}+4\pi\cdot d\left(1+\alpha^2\right)\right. \\ & -8\alpha\, sin\left(2\pi\cdot d+\arccos\left(\alpha\right)\right) \\ & \left.+sin\left(4\pi\cdot d+2\, arccos\left(\alpha\right)\right)\right). \end{aligned} \quad (20)$$

Compared to (3), (19) includes two extra variables: the transistor on-resistance R_{on} and the duty cycle d. For a given FET, the resistance R_{on} is usually obtained from the manufacturer's data sheet, but d needs to be solved, together with α from both (19) and (7).

For example, suppose we have a design set with I_p = 1 A, R = 1 Ω, and V_{DC} varying from 2 to 5 V (these are typical of transmitter designs). The duty cycle d can be solve numerically using *Mathematica*'s **FindRoot** function, as R_{on} increases (from 0 to 0.5 Ω) for various V_{DC}.

As shown in Fig. 4, when R_{on} = 0Ω, d is the same as calculated earlier [using only (3)]. As R_{on} increases, d also increases to compensate for the extra power loss on the transistor. The slope becomes steeper for decreasing V_{DC}. On the other hand, as long as the transistor power loss remains an insignificant portion of the total power output of the Class-E circuit, the increment of d is relatively small. In our experiences, for small duty cycles, on the order of 20%, the power loss on a typical transistor can be initially omitted in the design calculation.

IV. Design Examples

A. Simplistic Calculations

The current ratio α can be used to extract useful information for quickly accessing any Class-E circuit design. Given the following design set from the literature [13], f = 10.24 MHz, P_{out} = 72.2 mW, P_{DC} = 87.2 mW, R = 22 Ω, and V_{DC} = 2 V, we can calculate I_{DC} = P_{DC}/V_{DC} = 43.6 mA and $I_p = \sqrt{2P_{out}/R} = 81\ mA$. So the current ratio $\alpha = I_{DC}/I_p$ = 43.6/81 = 0.538. From Fig. 3, we know that α is approximately equal to d in this range. Or we can plug α = 0.538 into (8), the resulting duty cycle d equals 0.5, and this is confirmed by the use of 50% duty cycle in the original paper [13].

Note that the relation between the current ratio α and the duty cycle d does not depend on 100% power efficiency operation of the Class-E circuit, and in this particular case, P_{out}/P_{DC} = 82.8%.

The variables d and α also provide useful estimation of the upper bound of the coil current I_p, for any particular design. In theory, d_{max} = 1; thus α_{max} = 1. Assuming both 100% efficiency and that (2) is valid, we obtain $I_{p,max}$ from (3). In this case, the upper bound of the coil current $I_{p,max} = 2\ V_{DC}/R$ = 4/22 = 181.8 mA.

B. Step-By-Step Class-E Design Procedure

Given a primary coil inductance L = 25 μH, the objective is to design a high-efficiency Class-E circuit with the coil current amplitude I_p = 2 A. The other known design parameters are f = 470 kHz, V_{DC} = 5 V, Q_L = 155, and R_{on} = 0.04 Ω.

First, we assume that the transistor loss is not going to affect the duty cycle calculation, which can be justified later according to Fig. 4.

Under that assumption, we can use the simple algebraic equations (2)–(4) to calculate that the current ratio α = 0.096.

We can either use the explicit polynomial in (8) to calculate the duty cycle directly, d = 0.1814, or as comparison, solving the implicit equation (7), resulting d = 0.1816. The difference is quite small. In practice, the on-time of the transistor is usually adjusted in order to obtain the best combination of the desired coil current and the observation of the Class-E conditions. Since the duty cycle is less than 0.2, it justifies our omission of the transistor power loss at this stage of the design analysis, and avoids solving the two implicit equations (7) and (19) with the added parameter R_{on}. In fact, the *Mathematica* code solving (7) and (19) gives d = 0.1820, which, for our practical purpose, is close enough to the result of the explicit polynomial (8).

These α and d values can then be used in (11) to calculate C_{shunt}, and (15) to calculate C_{series}. The results are C_{shunt} = 103.6 nF and C_{series} = 4.77 nF.

A physical circuit was constructed using the results of the simplified design with 4.7 nF used for C_{shunt} and 100 nF used for C_{series}. The coil current i_p was measured with a Tektronix AC

current probe connected to an oscilloscope. The FET switch voltage v_s was also monitored on the oscilloscope (shown in Fig. 5). A potentiometer on the circuit board was used to adjust the duty cycle of the FET transistor gate drive pulse, such that $v_s(t)$ reached zero when the FET switch turned ON.

As shown in Fig. 5, the Class-E circuit is operating at the high-efficiency point; the measured versus specified design parameters are shown in Table I.

The bench-measured values are very close to the design targets.

C. Frequency Modulation of the Transmitter

Most often an implanted neural prosthesis requires transcutaneous control of its operation via commands sent over the same inductive link used for power transfer. To accomplish this, both amplitude [14] and frequency modulations of the Class-E converter are possible. In one method of frequency-shift-keyed operation, extremely rapid change of the transmitter operating frequency is employed [15], [16]. As shown in Fig. 6, an extra capacitor C_{fsk} in parallel with an extra transistor switch (*FSK*) can be added to the LC_{series} branch of the Class-E circuit. When that transistor is conducting, C_{fsk} is bypassed and the circuit is the same as the traditional Class-E circuit. When the transistor switch is open, C_{fsk} becomes in series with C_{series}, which changes the total capacitance, thus altering the operating frequency of the circuit. By turning the *FSK* transistor ON and OFF, at a strategic point in the Class-E cycle, we can modulate the frequency of the oscillating coil current while maintaining the low-loss, high-efficiency performance of the circuit.

As an example, for the same design specification in Section III-B, we can easily implement FSK modulation by varying the operating frequency *f*. The values of capacitors C_{shunt} and C_{series} can be calculated as before.

Fig. 7 shows a plot of the relationship between C_{shunt} and C_{series} for five coil currents using the Class-E design methods presented above. In Fig. 7, the data points of the same frequency are grouped by the ellipses: f_1 = 423 kHz, f_2 = 470 kHz, and f_3 = 517 kHz. These represent ±10% frequency modulation around 470 kHz. The straight lines connect the data points of constant coil current amplitude: I_1 = 1.7 A, I_2 = 1.8 A, I_3 = 2 A, I_4 = 2.2 A, and I_5 = 2.4 A. In theory, we can shift from one frequency to the other, provided that we change both C_{shunt} and C_{series} at the same time. In practice, the extra *FSK* transistor and C_{fsk} (see Fig. 6) effectively vary only C_{series}. So the design objective is to keep C_{shunt} constant, which is indicated by the horizontal dotted line in Fig. 7, while frequency modulating the coil current. The corresponding frequency *f*, C_{series}, I_p, and duty cycle *d* are collected in Table II.

In Table II, it shows that it is possible to have the values of C_{shunt} barely change, when C_{series} changes from 5.96 to 3.91 nF, by switching the FSK transistor, to produce the corresponding frequency shifts between 423 and 517 kHz. In this case, the circuit can be designed with the original capacitor C_{series} = 5.96 nF, and the added-on C_{fsk} = 11.37 nF. It also shows that theoretically to maintain high-efficiency operation at both frequencies, the duty cycle needs to change accordingly as well.

The FSK-modulated transmitter topology (see Fig. 6) is very simple and straightforward, but the numerical results reveal some possible issues with the coil current I_p changing from 1.7 to 2.4 A at two different frequencies. First, the FSK demodulators in some implants may be sensitive to the amplitude modulation of the magnetic field. Second, the change in I_p also causes I_{DC} to change from 125 to 307 mA. Since the dc current flows from the RF choke in series with the power supply, it cannot change instantaneously. As I_{DC} rebalances through the RF choke, it "blurs" the sharpness of the frequency modulation which causes the intersymbol interference in the FSK demodulator and could affect the inward data error rate.

It seems that it is best to operate on the equal-current lines in Fig. 7 to keep I_p constant. This is achievable by switching the values of both capacitors at different frequencies, a somewhat more complicated topology. Alternatively, the receiver coil in the implants may be tuned asymmetrically to the two modulating frequencies as a means of compensating for the different coil currents. One might choose to increase the coil current I_p at one frequency to "compensate" for the asymmetric frequency response of the demodulator in the implants. In any case, the calculation shows that by adjusting C_{shunt}, C_{series}, and duty cycle d, we have full control of the operation of the Class-E circuit for power and data transmission.

In our laboratory, numerous designs using the FSK modulation method have been implemented, and operational details have been reported [16]. A full mathematical analysis of the FSK modulation method will be presented in an upcoming publication as space does not permit a comprehensive treatment here.

V. Discussion

One might reasonably ask the question about how the design procedure presented here can be verified. Our derivation stems directly from first principles using fundamental energy balance and is mathematically equivalent to Raab's paper [3] on Class-E circuit analysis. However, his analysis provides very restricted design guidance and is difficult to apply except when the duty cycle $d = 0.5$. In contrast, the work presented here uses the D-OA approach that starts with the physical circuit elements most easily manipulated, and optimizes the duty cycle in order to satisfy the Class-E conditions.

In testing any new procedure, it would be comforting to have a "gold standard" for comparison. Unfortunately, there exist no other simple design procedures that incorporate the flexibility of our approach, particularly with respect to the duty cycle, and most other published methods involve intrinsic equations and numerical analysis. Yet, comparison to other published work is useful. Design and operational parameters from three Class-E circuit designs, spanning a Q-range of 7–340, are presented in Table III and compared to both our design approach and OrCAD simulations. The first is a textbook example using a 50% duty cycle; the others come from more complicated empirical approaches. For the first design, the textbook equations are mathematically equivalent to ours, and the resulting calculations demonstrate agreement. For the second design, although the authors in [17] do not report I_{DC} and α, our component values and simulation results agree with the published ones. For the third design, very close agreement is seen for all values.

Unfortunately many, if not most, Class-E circuit design procedures resort to 50% duty cycle as an *a priori* design parameter, for lack of manageable design equations. As shown in this paper, designing for a duty cycle other than 50% can be relatively easy using the D-OA approach. From a hardware implementation standpoint, 50% duty cycle is often undesirable due to the fact that the transistor switch then carries the resonant current for half of the cycle, and this causes excessive power dissipation in the switch due to its finite on-resistance. In our experience, designing numerous Class-E transmitters, restricting the duty cycle to a maximum of 20% produces minimal, to acceptable, switch power losses and maintains the high-Q approximation.

Our derivation used the high-Q approximation [5]. For many emerging neural prosthesis designs, such as the IMES [11], the relative size of the implantable device as compared to the transmitter coil is small, the coupling coefficient to the extracorporeal transmitter coil is correspondingly low, and there is minimal reduction of the circuit Q due to the loading of the implanted device upon the transmitter.

However, for other designs, owing to tighter coupling and reflection of the load, the loaded quality factor of the coil Q_L can be relatively low. It is instructive to consider whether the high-Q approximation could still be valid in these cases. A lower Q_L will result in a lower series branch Q and the expectation that notable power would be contained within higher harmonics. Higher order Fourier transforms can be computed for the shunt capacitor voltage $v_s(\theta)$ and the "leaked" power can be examined at those higher harmonics. This harmonic leaked power is exacerbated by the use of 50% duty cycle.

In keeping with simplicity, a relationship between L, Q_L, I_p, and α can be derived as in (21). Using this expression, choices can be made for V_{DC} and L in order to change the circuit Q. Once the other design parameters are specified, Q_L and α are inversely proportional, and (21) can be used as a guideline for choosing the appropriate Q_L:

$$\frac{I_p}{2V_{DC}}\omega L = Q_L \times \alpha. \quad (21)$$

As an example, to improve the previously presented textbook design [18, Example 5.1], the coil Q_L could be increased by a factor of 5, and thus, $Q_L = 35$ and $\alpha = 0.537/5 = 0.107$. That could drop the duty cycle to 19% and the corresponding $C_{shunt} = 1.47$ nF and $C_{series} = 312$ pF.

As derived from our experience, to keep the high-Q approximation valid, one needs to limit the current ratio $\alpha < 0.2$, and from (21), that amounts to (22)

$$Q_L > 2.5\frac{I_p}{V_{DC}}\omega L. \quad (22)$$

In one application [11] with $I_p = 2$ A, $V_{DC} = 5$ V, $f = 400$ kHz, and $L = 25$ μH, the quality factor of the coil Q_L needs to be larger than 63 for a high-Q approximation Class-E design.

VI. Conclusion

This paper presents the detailed derivation of explicit design equations for the current-mode closed-loop Class-E circuit at any duty cycle. The derivation uses the same assumptions as those in the classical Class-E power amplifier. In addition, it takes into account the power loss due to the on-resistance of the transistor.

Because the derivation does not include the nonlinear transistor capacitance model, or finite dc feed inductor, only one intermediate variable, i.e., the current ratio α, is introduced. It is related to the duty cycle d via the ZVDS condition. The current ratio also appears in the power balance equation.

Maintenance of the correct Class-E frequency is crucial for viable hardware designs. Deviation from the correct frequency can cause rapid destruction of the transistor switch due to excessive power dissipation, especially for high-Q designs which contain large stored energy. Simultaneously satisfying the ZVDS and the ZVS conditions is a necessary criterion for deriving the correct frequency, and these are obtained through the combined use of the design process presented here and the closed-loop control [5].

The current-mode closed-loop control desensitizes the high-efficiency Class-E circuit to the variations of its components. Using the closed-loop control, the transistor inherently turns ON at the zero-crossing point of the coil current, the circuit automatically satisfies the ZVDS condition, or optimizes the onset of switching for lower-Q circuits. Therefore, the design problem becomes essentially to size C_{shunt} and C_{series} in order to meet the ZVS condition. The explicit formulas for both capacitors involve the current ratio α, resulting in the determination of the duty cycle d, which is an easily adjusted parameter for a Class-E system.

The design process presented here can easily be implemented in a spreadsheet or a dedicated design program. For demonstration, an online design calculator, incorporating these design equations, can be found at http://class-e.sigenics.com.

Biography

Philip Troyk (M’83–SM’91) received the B.S. degree in electrical engineering from the University of Illinois at Urbana–Champaign, Champaign, and the M.S. and Ph.D. degrees in bioengineering from the University of Illinois at Chicago, Chicago.

He is currently a Faculty Member in the Department of Biomedical Engineering, Illinois Institute of Technology, Chicago, where he also serves in the capacity as the Associate Dean

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Zhe Hu received the B.S. degree in electrical engineering and the M.S. degree in biomedical engineering from Tongji University, Shanghai, China, in 1999 and 2002, respectively, and the Ph.D. degree in biomedical engineering from the Illinois Institute of Technology, Chicago, in 2008.

He is currently a Senior Biomedical Engineer at Sigenics, Inc., Chicago, IL, where he regularly applies the design-oriented circuit analysis and measurement techniques to his research and development tasks.

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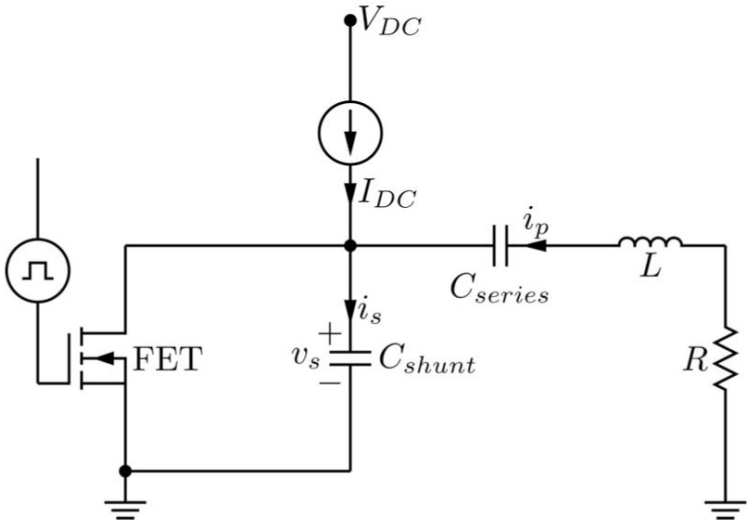

Fig. 1.
Class-E circuit diagram.

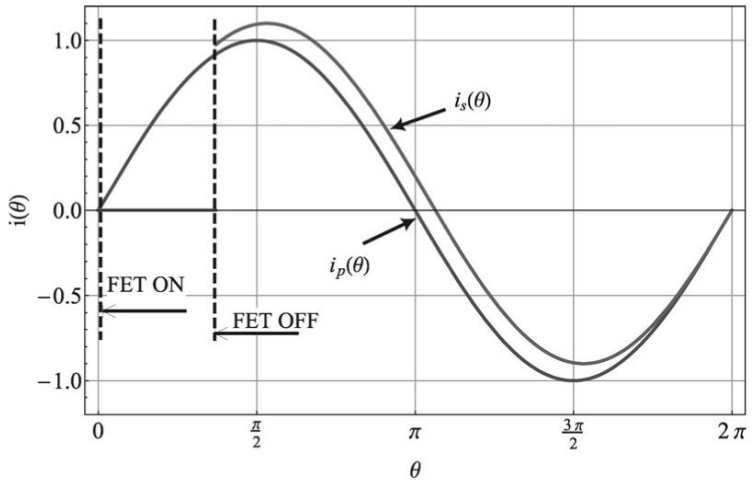

Fig. 2.
Coil current i_p and capacitor current i_s waveform; $d = 0.186$ and $\alpha = 0.1$.

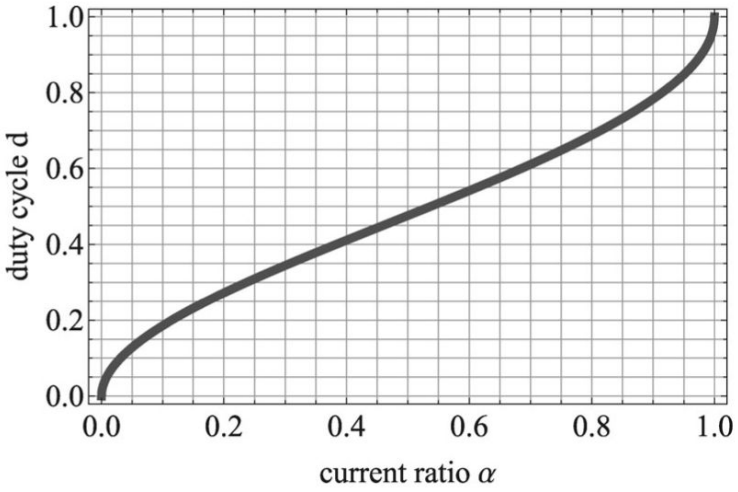

Fig. 3.
Duty cycle as a function of current ratio.

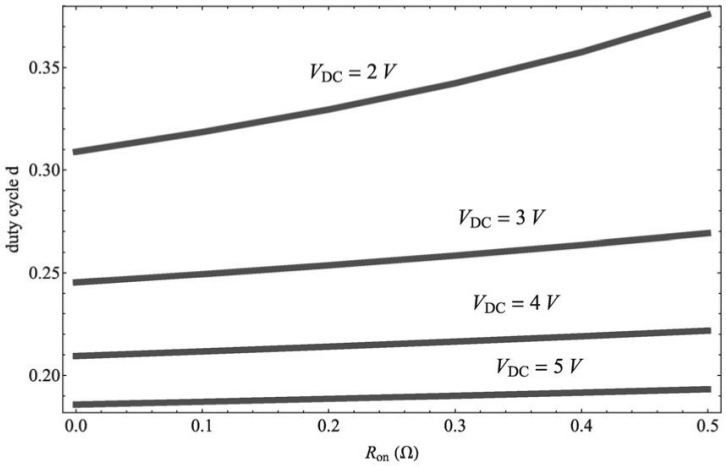

Fig. 4.
Duty cycle as a function of on-resistance.

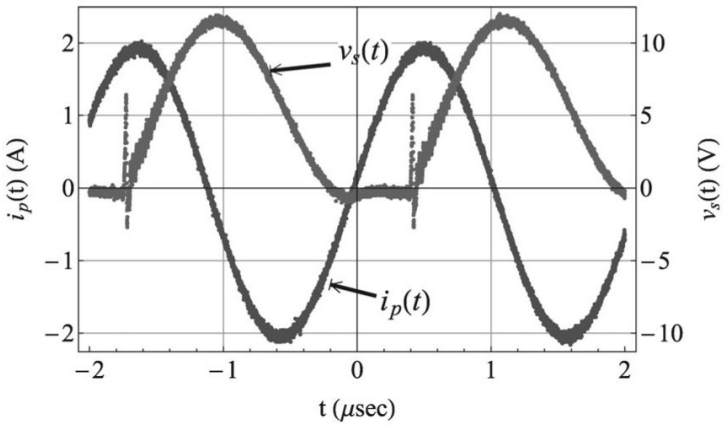

Fig. 5.
Coil current and switching voltage scope capture at duty cycle 18%.

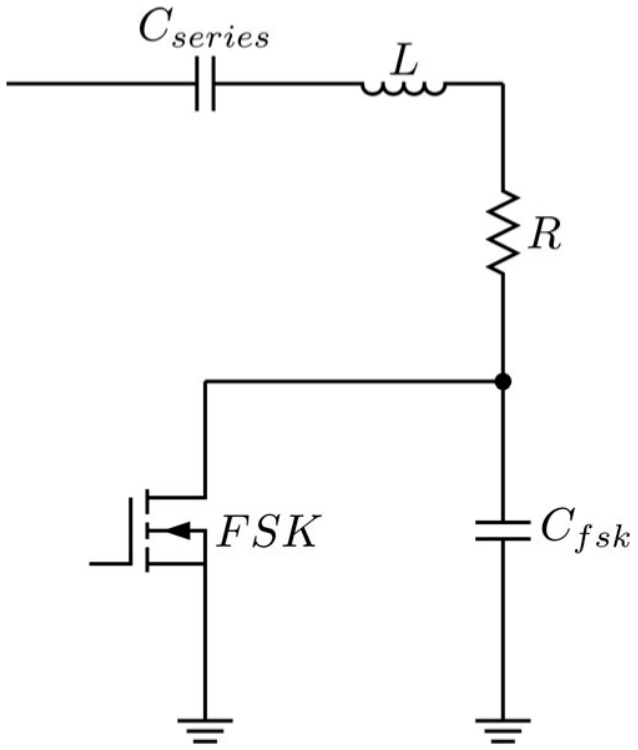

Fig. 6.
Frequency modulation circuit.

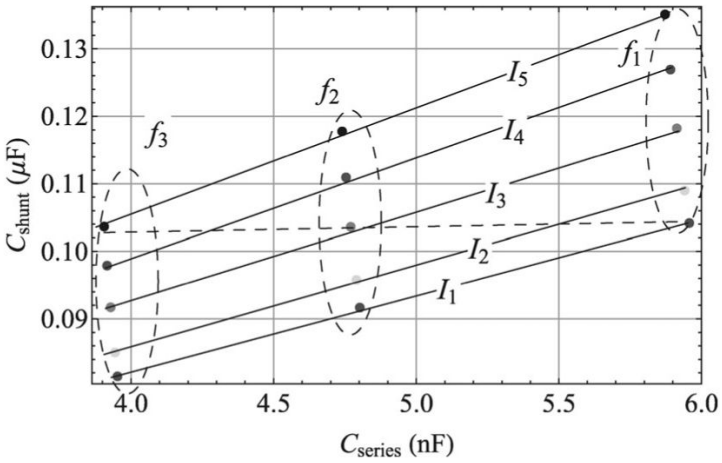

Fig. 7.

C_{series} and C_{shunt} values at different frequency f and I_p .

TABLE I

Specified, Simulated, and Measured Parameters

	f (kHz)	I_p (A)	I_{DC} (mA)	V_{DC} (V)	L (μH)	Q_L	duty cycle d	C_{shunt} (nF)	C_{series} (nF)	power efficiency
specified	470	2	190	5	25	155	0.18	103.9	4.77	100%
OrCAD simulation	469.5	2	194	5	25	155	0.18	103.6	4.77	98%
measured	471	2	201	5	25	155	0.18	100	4.70	95%

TABLE II

Design Parameters for Frequency Modulation

f (kHz)	C_{series} (nF)	C_{shunt} (μF)	I_p (A)	d	α	I_{DC} (mA)	switch-on time (ns)
f_1 = 423	5.96	0.1042	I_1 = 1.7	0.158	0.073	124	374
f_2 = 470	4.77	0.1036	I_3 = 2.0	0.182	0.096	192	387
f_3 = 517	3.91	0.1037	I_5 = 2.4	0.212	0.128	307	410

TABLE III

Design Parameters in the Literature Comparing to Our Calculation

design in the literature		design parameters (input)						calculated values (output)			
		f	I_p (A)	I_{DC} (A)	V_{DC} (V)	$L(\mu H)$	Q_L	current ratio a	duty cycle d	C_{shunt}	C_{series}
1	literature [18]	1.2 MHz	1.49	0.8	100	66.9	7	0.537	0.5	337.4 pF	314.6pF
	our calculation	1.2 MHz	1.49	0.8	100	66.9	7	0.537	0.5	338 pF	314.8pF
2	literature [17]	800 kHz	0.44	-	4.5	27.2	13	-	0.5	3.755 nF	1.881 nF
	our calculation	800 kHz	0.44	0.23	4.5	27.2	13	0.51	0.49	3.69 nF	1.61 nF
	OrCAD simulation	800 kHz	0.44	0.23	4.5	27.2	13	0.51	0.50	3.69 nF	1.61 nF
3	literature [19]	189.7 kHz	0.46	0.25	4.0	2637	340	0.537	0.5	16.46 nF	268 pF
	our calculation	189.7 kHz	0.46	0.24	4.0	2637	340	0.532	0.5	16.9 nF	267.8 pF
	OrCAD simulation	189.7 kHz	0.48	0.27	4.0	2637	340	0.56	0.50	16.9 nF	267.8 pF