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# Lifetime-based Power Routing in Parallel Converters for Smart Transformer Application

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**Abstract**—The use of a Smart Transformer-based electrical distribution could be an effective approach to reorganize the electric grid, solving the problems and challenges of distributed generation systems and active loads. While lower efficiency and higher cost compared to the conventional transformer are well known and investigated limiting factors, the required higher maintenance, related to the use of electronics systems in the electric grid, is seldom targeted. In fact, high maintenance cost would make the use of Smart Transformer inapplicable even if new services could justify higher initial cost and new semiconductor development could increase the overall efficiency. This work proposes a modular repairable system based on condition monitoring, which aims at equalizing the lifetime consumption of the single modules to make possible prognostic maintenance.

## I. INTRODUCTION

The continuous increase of grid connected renewable energy systems and the consequently fast-changing power flow in the electrical distribution grid is challenging the current grid configuration. Additionally, new loads, such as electrical vehicle charging stations, absorb peak power, which complicates the control of the grid nodes and calls for new concepts to overcome the related problems [1]. Among different solutions, the Smart Transformer (ST) as the link for the medium-to-low-voltage (MV/LV) distribution would allow a slow transition towards more intelligent low-voltage grids, while still retaining the backwards compatibility with existing equipment used in the actual grid [2]. The availability of DC links in MV and LV side of the ST allows to decouple the grids and to provide services to both AC grids. By controlling the amplitude of voltage, the load consumption can be controlled [3], while the frequency variation can act on the droop control of the generators in the grid, which can also be used to prevent reverse power flow in the grid [4].

The main challenges for a ST are the efficiency and the reliability, as the standard low-frequency passive transformers set the reference levels to very high targets. In literature works addressing the reliability of modular power converter structure can be found [5], and the findings support the thesis that

modular architectures allow increasing the efficiency. During partial load operation, the efficiency can even be optimized by controlling the number of activated/deactivated modules [6]. However, the deactivation process of a module is complex and requires special attention to remain in the safe operation area of the power semiconductors, which is realized with special gate drivers in the cited work. Furthermore, the power quality is compromised by an increased current ripple in the output current and the capacitors, if the converters are operating in interleaved operation. So the activation/deactivation of modules achieves an increase of the efficiency at the cost of power quality deterioration, uneven lifetime consumption of the overall system and lower reliability.

In a modular architecture with many cells, it is reasonable that when a cell fails, the cell is replaced and sent to maintenance irrespective of the failed components. The same cell is repaired and becomes available as a replacement unit. Eventually, a ST modular system is composed of differently aged cells [7].

To overcome the problem of different remaining lifetimes of the power electronic modules, this work proposes to take advantage of the modularity of the system in another way. The proposed approach is not to shut down modules, but to route the power along different paths in partial load operation [7], [8], [9]. This enables to control the lifetime of the system and to extend the operation time for modules with high accumulated damage, which can be estimated with condition monitoring techniques. The goal is to let the weaker modules survive until the next maintenance is made, stressing them less compared to the stronger ones. Given these premises, the power is shared among the modules depending on the consumed lifetime. Moreover, the consumed lifetime estimated to implement this power routing can also be used to schedule prognostic maintenance.

The paper is organized as follows: Section II describes the concept of condition monitoring. In section III the power routing is introduced and in the following section IV the system and the controller implementation is explained. An experimental validation is made in section V before the conclusion is drawn in section VI.

## II. CONDITION MONITORING OF POWER ELECTRONICS CONVERTERS

For the reliability analysis of the system, pure statistics are not sufficient; the failures need to be traced back to their physical root cause, referring to the physics of failure approach [10].

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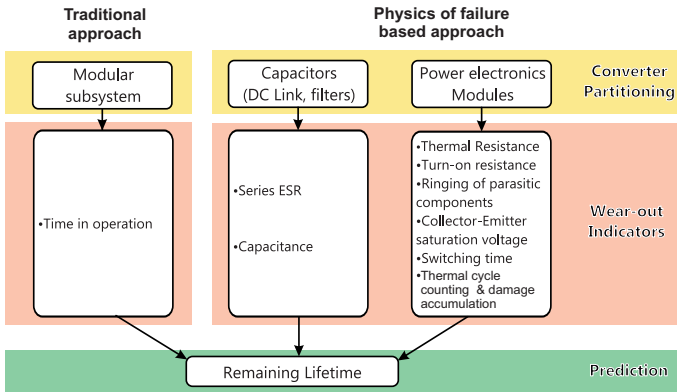


Fig. 1: Condition monitoring for power electronic converters.

Due to the high number of components in power electronic converters, first the most frequently failing components need to be identified. In literature it has been reported that these are the capacitors and the power semiconductors [11], [12]. This paper focuses only on the failures caused by semiconductors. The physics of failure concept used for the reliability analysis can be utilized for a lifetime prediction. As an example for power semiconductors, the manufacturers provide the time to failure by the number of thermal cycles to failure  $N_f$ , which is expressed in (1), where  $\Delta T$  is the magnitude of the thermal swing, whereas  $T_{j,av}$  is the average junction temperature during this swing and  $a_1$ ,  $a_2$  and  $a_3$  are fitting parameters.

$$N_f = a_1 \cdot (\Delta T)^{a_2} \cdot e^{\frac{a_3}{T_{j,av} + 273^\circ C}} \quad (1)$$

Unlike the power cycling tests, where  $\Delta T$  is constant, the mission profile of an ST based smart grid is not deterministic and hence a cycle counting method is required to decompose the temperature profile. The rainflow algorithm is one of the widely employed cycle counting method for fatigue analysis [13]. Subsequently, Miner's rule can be applied to calculate the accumulated damage using [14]

$$D_{acc} = \sum \frac{N_i}{N_{fi}} \quad (2)$$

where  $D_{acc}$  is the accumulated damage,  $N_i$  the number of detected cycles in the  $i$ -th stress range and  $N_{fi}$  the number of cycles to failure of the  $i$ -th stress range. When the accumulated damage becomes 1, the device fails. It is assumed that the damage accumulates linearly.

Furthermore, there are parameters in the system, which correlate with the degradation. Using real time measurement system for monitoring these parameters is referred to as condition monitoring. By employing condition monitoring with health prognostics, this enables to schedule the maintenance and replacements before a component fails and thus prevents down times of a system.

For health monitoring in power electronic converters, the possible parameters which can be used as indicators for the condition monitoring are shown in Fig. 1. Here, the system is grouped into smaller parts to enable the desired model

precision in the estimation of the remaining lifetime. The simplest form is to measure the time in operation with the assumption that the oldest part fails first. This approach lacks of physical background, but is commonly applied in the industry to schedule maintenance of components. The strongest advantage is that no additional sensors are required, while it is simple and does not cause errors due to wrong measurements.

For a better lifetime estimation, the components, which are prone to fail first, need be identified and their related failure mechanisms need to be investigated. As pointed out before, critical components for power converters are capacitors and power semiconductors. Condition monitoring for electrolytic capacitors is possible by monitoring the series ESR and the capacitance of the capacitors, which can be implemented for real time application [15]. For power electronics, condition monitoring is extremely complex because of the various possible failure mechanisms and the various possible parameters, which can be monitored. Different parameters such as Collector-Emitter saturation voltage  $V_{ce}$ , IGBT turn on resistance, thermal resistance, gate signals, switch times etc. can be used to estimate the lifetime of the power semiconductors [16]. Among these techniques,  $V_{ce}$  measurement will be a standard in high power converters since they can also be used to monitor the junction temperature for avoiding trivial failures [17]. The failure criterion to define the end-of-life for the component for the  $V_{ce}$  measurement is already well established [18]. This  $V_{ce}$  measurement can be used for the sensing of the junction temperature and thermal cycle counting & damage accumulation as expressed with (1)-(2).

A comprehensive work including the condition monitoring and prognostics for the lifetime of power semiconductors has been made in [19]. The work demonstrates a lifetime estimation technique based on accelerated lifetime tests.

### III. POWER ROUTING IN MODULAR POWER CONVERTERS

With respect to the state of the art, turning off one or more redundant converters is applied to improve the efficiency during partial load operation [6]. This deactivation changes the stress distribution in the system and impacts the power quality in terms of current and voltage ripple. Consequently, the operating converters are loaded higher, which leads to more severe thermal cycles. Since thermal cycles are the main cause of aging in power electronic modules, the module, which is turned off is relieved from the stress induced by the mission profile. As a consequence, the thermal stress for those parts of the system, which continue to operate, is increased. This leads to an unequal expected remaining lifetime of all parts. Instead of turning parts off, the concept of power routing operates the power converter under unequal loading conditions for the maximization of the time to the next maintenance [7].

Routing the power can reduce the thermal stress caused by power cycling during normal converter operation for specific parts of the system. This can follow the target of stress reduction for specific parts of the power converters, e.g. when one parallel converter is suffering from wear out and has a low remaining lifetime with respect to the others. For an optimization, the information obtained from the condition monitoring

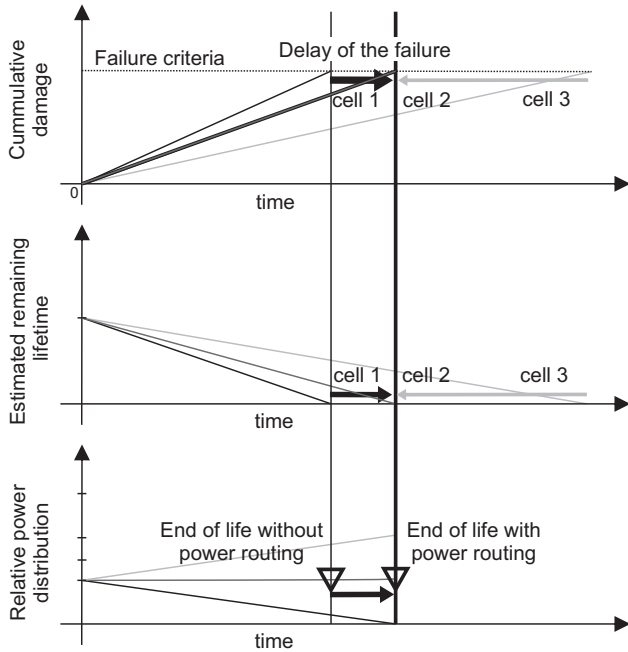


Fig. 2: Demonstration of the power routing concept for three redundant power paths with different lifetimes with power routing for extending the time to the next failure.

is used and applied to control the lifetime of all parts in the system. This is demonstrated in Fig. 2. The accumulated damage is used as the parameter for the determination of lifetime for the three converters [20]. Here, the failure criteria is when the accumulated damage becomes unity. The aging is demonstrated as it is commonly done without modifying the power distribution in the system with thin lines. Consequently, the end-of-lifetime (ELT) happens when the first converter is failing. The concept of the power routing is demonstrated with bold lines, while the difference is highlighted with the arrows. The different lifetimes of the cells are used to route the power in the way, that the converter, which would naturally fail first, is unloaded, while the other converters with longer expected lifetimes are loaded higher. As a consequence, the failure can be delayed and during the next maintenance one or more parts can be substituted.

However, the converters are not oversized for the power routing. In case of the above example with three parallel cells, the maximum current  $I_{1,out,max}$ , which one cell can transfer is limited by its rated current. For unloading one cell, the minimum current is dependent on the number of parallel converters  $n_p$  and the overall output current  $I_{out}$ . This is expressed in (3).

$$I_{1,out,min} = \begin{cases} 0 & \text{if } (n_p - 1) \cdot I < I_{out} \\ I_{out} - (n_p - 1) \cdot I, & \text{otherwise} \end{cases} \quad (3)$$

With this equation, it can be shown, that in a converter with three cells  $n_p = 3$ , one cell can be completely unloaded

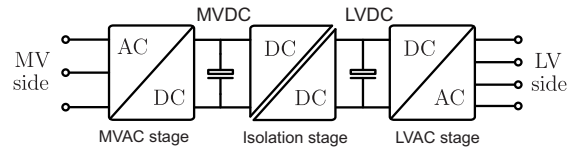


Fig. 3: Schematic architecture of the three-stage ST.

up to 66.7 % of the rated current. The more general form in dependence of an arbitrary number of unloaded cells is expressed in (4).

$$I_{n_{un},out,min} = \begin{cases} 0 & \text{if } (n_p - n_{un}) \cdot I < I_{out} \\ \frac{I_{out} - (n_p - n_{un}) \cdot I}{n_{un}}, & \text{otherwise} \end{cases} \quad (4)$$

Based on this equation, it can be shown, that two cells can be completely unloaded up to  $0.33 I_{out}$ .

In the following, the power routing concept will be presented with the application of virtual resistors in parallel power converters. The impact of virtual resistance based power routing on the lifetime of the converter system is quantitatively investigated. Moreover, the variation of estimated lifetime with different virtual resistance algorithms are also presented.

#### IV. STUDY ON THREE PARALLEL CONVERTERS IN THE LV STAGE

This section introduces the system on which the power routing is demonstrated and the implementation of the algorithm in the controller.

##### A. ST Architecture

With the motivation for services in the distribution grid, a three-stage ST architecture in Fig. 3 is the most likely configuration [21] and it is chosen as a reference in this paper. Each stage controls a specific variable: the LV converter implements a voltage closed-loop control, to ensure grid waveforms with low Total Harmonic Distortion (THD), while the DC/DC converter controls the Low Voltage Direct Current (LVDC) link voltage, ensuring a stable supply for the LV converter. The DC/DC converter also performs the balancing of the MV cells. Finally, the MV converter implements the Medium Voltage Alternating Current (MVAC) closed loop current control, in order to regulate the total Medium Voltage Direct Current (MVDC) link, which is providing the power for the isolation stage.

##### B. System description of three parallel power converters

The LV stage of the ST is forming the LV grid and consists of three parallel converters as schematically shown in Fig. 4. The converters require access to the fourth wire, because of the numerous single phase loads in the grid. Using the two level voltage source converter, as it is commonly done for motor drives, enables to add a fourth half bridge to the converter as it is shown in Fig. 5. This half bridge is connected to

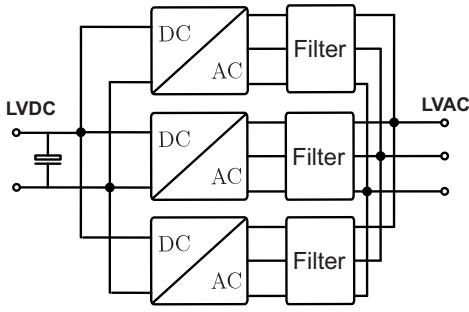


Fig. 4: System of three power converters for the LV stage.

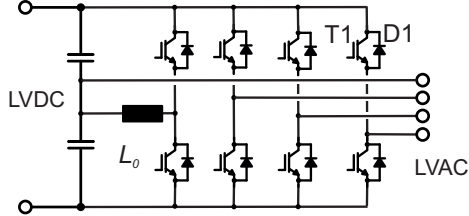


Fig. 5: Topology of one two level VSI.

the star point of the DC link for preventing high common mode voltages. The loading of the power semiconductors is symmetrical over time, which requires to only investigate the effect on one IGBT T1 and one Diode D1 in a half bridge.

Since the ST operates at partial load for most of the time as shown in the Fig. 6, the parallel converters allow redundancy at partial load operation. However, since there is no oversizing of converters, all the converters are required to cater the full power operation. The possibility of interleaved operation of the converters enables a reduction of either the switching frequency or the filter size in comparison with a single power converter. Apart from the advantages of parallel converters, there are issues, such as circulating currents if a shared DC link is used for the three converters [22]. However, this is not the scope of this work and the known solution to use single phase inductors for each converter is applied to overcome this problem.

### C. Control of the power in the LV stage

The LV stage converter of the ST needs to form the grid voltage of the connected LV grid. As a consequence, the shape of the grid voltage needs to be controlled and the active power depends on the connected loads. Thus, the ST needs to control the voltage in an outer control loop and the current in an inner control loop. However, only the current control is investigated in this work due to its importance for the power routing. The implementation of the power routing in the current controller is shown in Fig. 7. The virtual resistors are used to route the power similar to current divider in the basics of electronics by distributing the current references for the three converters. A closed loop control for the power routing is necessary to prevent power circulation among different converters.

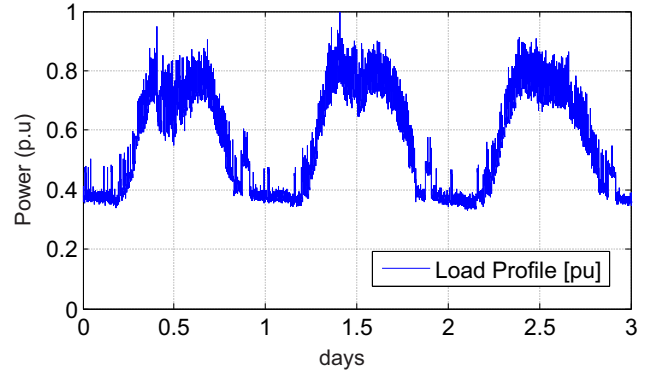


Fig. 6: Example for a mission profile of an ST fed micro-grid.

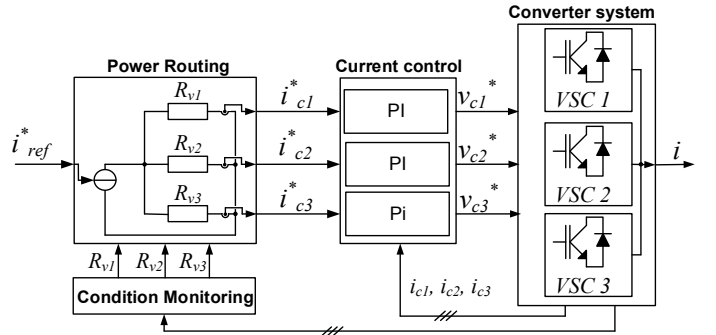


Fig. 7: Control diagram of the power routing algorithm based on condition monitoring.

To define how the power is routed in the system, the virtual resistors need to be tuned based on the condition of the converters in the parallel power paths. A high resistance of a path leads to low loading and a low resistance leads to high loading of the path. For similar conditions of the converter, the power needs to be distributed equally and all virtual resistors need to have the same size. As an example for the current transferred in converter 1,  $i_{c1}^*$ , is dependent on the overall reference current generated by the voltage controller  $i_{ref}^*$  and all virtual resistors in the parallel paths. This is shown in (5).

$$i_{c1}^* = i_{ref}^* \cdot \frac{R_{v2}R_{v3}}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}} \quad (5)$$

The power routing for all three reference currents is shown in a matrix representation in (6).

$$\begin{bmatrix} i_{c1}^* \\ i_{c2}^* \\ i_{c3}^* \end{bmatrix} = \frac{i_{ref}^*}{R_{v2}R_{v3} + R_{v1}R_{v2} + R_{v1}R_{v3}} \begin{bmatrix} R_{v2}R_{v3} \\ R_{v1}R_{v3} \\ R_{v1}R_{v2} \end{bmatrix} \quad (6)$$

It needs to be pointed out, that the power routing does not require an oversizing of the converter system. In case that a converter receives a higher current reference than the maximum current, the power exceeding the limit is redistributed for the other converters. Consequently, under full load every

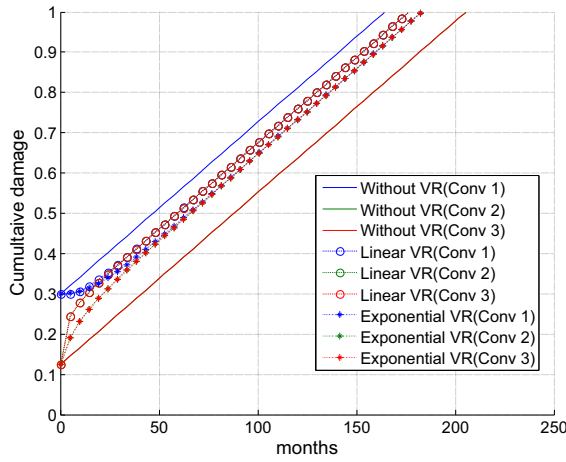


Fig. 8: Case 1: Variation of accumulated damage of parallel converters with and without Virtual Resistor (VR) power routing.

single converter is processing the rated power, independently from the tuning.

#### D. Design of Virtual Resistor based Power Routing

In order to establish the relation between the virtual resistance and estimated lifetime of the converters, first, a simplified electro-thermal model of the parallel converters is developed in MATLAB. The mathematical model consist of the two-level converter equations along with thermal model of the power semiconductor and heatsink for evaluating the semiconductor losses, and thereby the junction temperature. Using this simplified mathematical model, the junction temperature of the semiconductors can be calculated for any mission profile. The heatsink and power semiconductors are chosen and designed to have an estimated lifetime of 20 years for the semiconductor modules.

The number of cycle to failure can be calculated from the junction temperature using (1). Since the mission profile of an ST is not deterministic, the Rainflow algorithm is used as the cycle counting method and Miner's rule (2) is applied to calculate the accumulated damage.

The virtual resistor based power routing algorithm uses the sensed junction temperatures  $T_j$  of the power semiconductors to estimate the accumulated damage of each converter for a fixed time period. This accumulated damage gets updated after a fixed time period as expressed in (7).

$$D_{acc} = D_{acc,old} + D_{period} \quad (7)$$

The virtual resistors, which facilitate the power routing are expressed as a function of the accumulated damage as in (8). In order to define the function,  $f(D_{acc})$ , a linear (9) and an exponential relationship (10) are tested. The parameter  $\alpha$  and  $\beta$  depends on the coefficients  $a_1$  and  $a_2$  since (10) is derived from (1) considering  $D_{acc} = f(N_f)$ ,  $\Delta T = f(I)$  and  $I = f(R_{vi})$ .

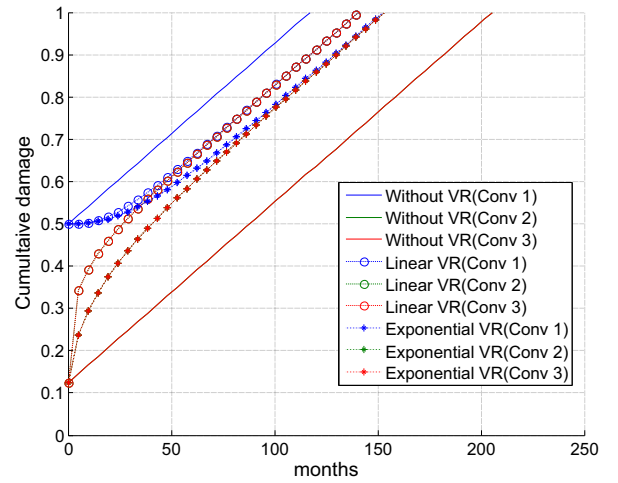


Fig. 9: Case 2: Variation of accumulated damage of parallel converters with and without Virtual Resistor (VR) power routing.

The linear function is used to limit the calculation effort and for easy implementation.

$$R_{vi} = f(D_{acc}) \quad (8)$$

$$R_{vi} = D_{acc} \quad (9)$$

$$R_{vi} = \alpha \cdot (D_{acc})^\beta \quad (10)$$

*Parallel converters with different initial accumulated damages:* A case study to establish the relation between the accumulated damage and virtual resistance and its effect on aging of converters is carried out in this section. For this analysis, a three day mission profile of an ST fed micro-grid, as shown in Fig. 6, is considered [23],[24].

First, the three converters are fed with balanced power distribution, irrespective of the initial accumulated damages, the accumulated damages and end-of-lifetimes are calculated. Then virtual resistors are introduced according to (9)-(10) and the accumulated damages and ELTs are calculated.

Three cases with different initial damages for each converter are considered here. Fig. 8, 9, 10 show the damage accumulation over the years for a modular converter system with different initial damages for cases 1 – 3. It is evident that without power routing, the converters will fail at different time instants. With virtual resistor method, the accumulated damages converge resulting in the control of processed power dependent failure of the system. The impact of power routing on the lifetime extension of the total system of the cases 1–3 is summarized in Fig. 11. The exponential function describes the relation between damage and virtual resistors more accurately and hence the ELTs of are better compared to the linear one in all three cases. The percentage increase in the total estimated lifetime of the system is depicted in the Fig. 11. In all the cases with different initial estimated lifetimes, there is an increase in the total estimated lifetime of the system up to 44%.

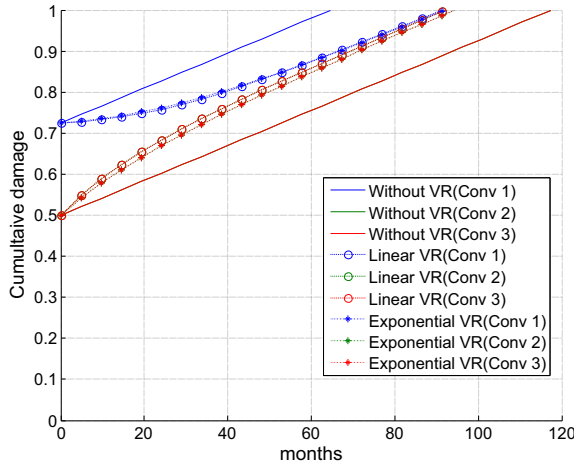


Fig. 10: Case 3: Variation of accumulated damage of parallel converters with and without Virtual Resistor (VR) power routing.

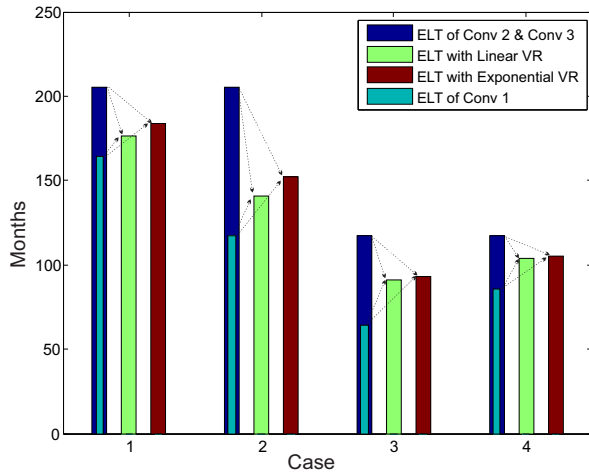


Fig. 11: Estimated lifetime (ELT) of parallel converters with and without virtual Resistor (VR) power routing for different cases.

It is assumed that the modular system reaches its ELT when the module with the lowest ELT fails. The results clearly show that the virtual resistors can increase the lifetime of the most aged cell and most importantly, decrease frequent maintenance schedules. However, it is evident that the increase in ELT of the system comes at the expense of lowering the ELTs of the higher loaded cells.

*Parallel converters with different thermal characteristics:* To validate the performance of virtual resistors for a parallel converter system with different thermal characteristics, a case study is performed. Here, all converters are assumed to have identical initial accumulated damages. Due to the difference in thermal characteristics, the converters have different ELTs, which is shown as case 4 in Fig. 11. Here, the heatsink temperature of one of the parallel converters is assumed to be  $5^{\circ}\text{C}$

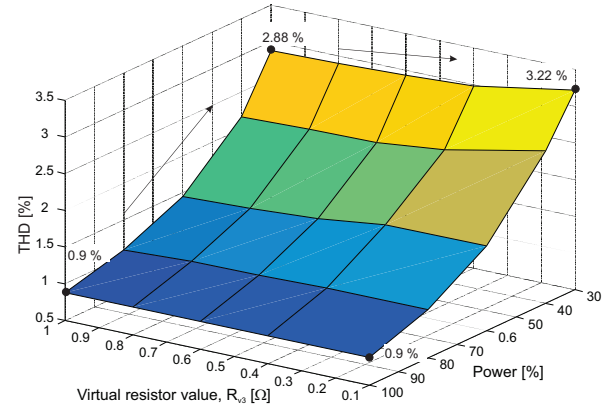


Fig. 12: THD variation of line current with virtual resistance unbalance for entire power range. The virtual resistance of converter 1 and converter 2 is normalized to  $R_{v1} = R_{v2} = 1 \Omega$ .

higher than that of the others. This is a reasonable assumption since the heatsinks are cooled with air/water entering from one end and leaving at the other, resulting in an uneven distribution of the heat. The ELTs of the converters without power routing are 86 and 117 months for the converter with higher heatsink temperature and others respectively. A significant increase of the total lifetime of the system of 22% or 19 months is obtained with the virtual resistor based power routing. Thus, the power routing strategy does not only increase the reliability of systems with different initial aging, but also for systems with different thermal behavior.

It can be concluded from the case studies that the linear and exponential functions of virtual resistors provide comparable results. The linear function does not require any tuning based on the expected mission profile of the system, which makes the implementation simple and straightforward. The exponential function instead offers one more tuning parameter, which can be tuned based on the expected mission profile and the remaining useful lifetime of the other parts to control the convergence time of the different lifetimes.

*Effect of power routing on line current ripple:* To demonstrate the effect of a power unbalance on the line current ripple and consequently the THD, a simulation study with unbalanced virtual resistors is carried out. Two of the three virtual resistors are constant  $R_{v1} = R_{v2} = 1 \Omega$ , while the third one is varied to show the effect on the current ripple. The result is illustrated in Fig. 12, where the x-axis shows the output power and the y-axis shows the virtual resistor of converter 3. For a  $R_{v3} = 1 \Omega$ , the system is operated under balanced condition and as the value decreases, the power distribution changes according to (6). The THD (in %) is shown on the z-axis. As expected, the THD of the line current increases for a reduction of the output power. For an increasing power imbalance, an increase in the THD of the output current can be seen. Under full load, this does not occur, because the power is equally distributed in the converters in order to prevent oversizing of components.

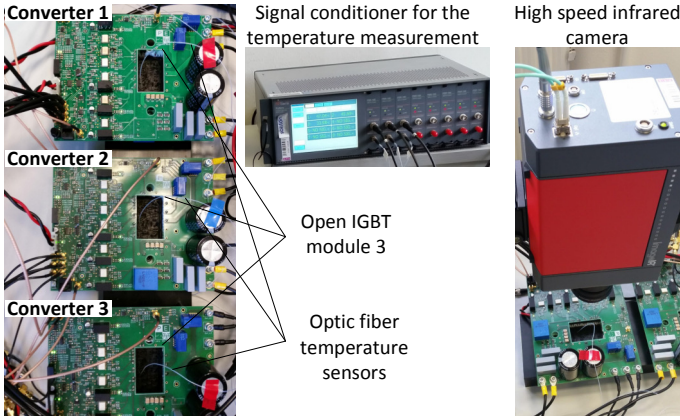


Fig. 13: Picture of the setup showing the three parallel converters assembled on one heat sink, a signal conditioner for the fiber optic temperature sensors and high speed infrared camera for junction temperature measurement of a full power electronic module.

TABLE I: Parameters of the laboratory setup.

Rated current per converter	25 A
DC link voltage	200 V
Filter size	1.8 mH
Load $R$	3.5 $\Omega$
Fundamental frequency	50 Hz
switching frequency	20 kHz
Power Semiconductor module	Danfoss DP25H1200T101667 – 10166

## V. EXPERIMENTAL VALIDATION OF POWER ROUTING

This section validates the concept of power routing on the experimental setup shown in Fig. 13. The three parallel converters with open IGBT modules share the same DC link and have single phase inductors at the output of each phase. The IGBT modules are not filled with gel for direct measurement of the junction temperature, which is reducing the voltage blocking capability of the power module. However, the removal of silicone gel does only marginally affect the thermal behavior, because the thermal conductivity of silicone gel or air is very low. A three phase resistive load is fed by the converters and the parameters of the setup are shown in Table I. First, the impact of unequal loading of parts of the system is demonstrated afterwards the efficiency impact of the power routing is demonstrated with power analyzer measurements.

### A. Reliability impact of power routing

In this subsection, the effect of unequal loading on the junction temperature of the converter is investigated. The junction temperature of the power semiconductors is measured with a special optical fiber instrument and this enables to measure the junction temperature with the open modules shown in the setup.

The infrared camera is used to detect the hottest spots in the power electronic module. The hotspot is affected by the self-heating of the chip as well as by the thermal cross coupling

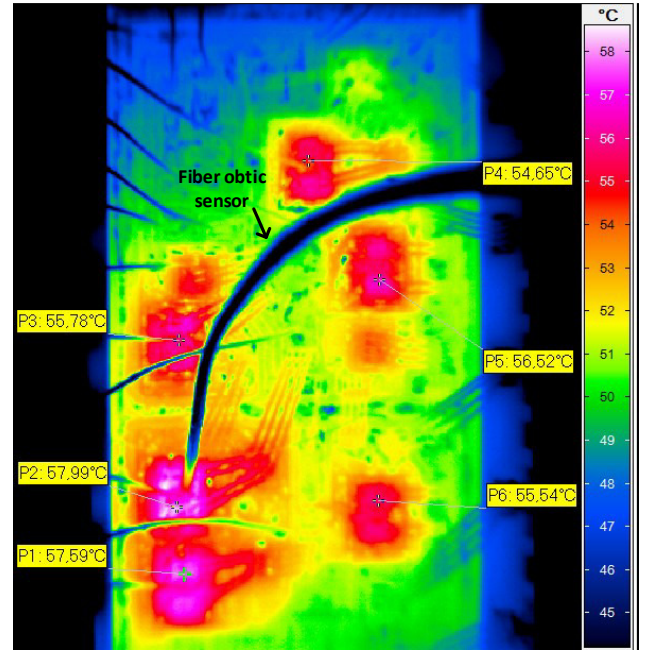


Fig. 14: Infrared camera picture of the power electronic module showing the thermal distribution of a full power electronic module highlighting the temperature on the IGBTs.

between the power semiconductors. An image of the power electronic module is shown in Fig. 14. It can be seen that the chips are hotter than the bond wires. Furthermore, the power semiconductors, which are located close to each other obtain the hottest chip temperature. The highest temperature is indicated with the measurement point "P2" and measures the temperature of IGBT 1. For this reason, in each of the converter the junction temperature of the IGBT T1 is measured. For the demonstration of the unequally loaded devices, the three converters feed constant current and the current distribution is varied slowly as shown in Fig. 15. Initially, converter 3 is loaded less than the other two converters and through a variation of the virtual resistor, all converters are loaded equally at  $t = 20$  s. Afterwards, converter 3 is loaded higher, while the other two converters are unloaded. The virtual resistors are varied again to achieve equal power transfer and then converter 3 is loaded higher. From the reference current, it can be seen, that the power is routed according to the virtual resistors as desired. The measured currents are in accordance with the reference value. However, even more important is the visible effect on the junction temperature. During equal loading of the converters, the junction temperature is approximately equal, but unloading a part leads to a reduction in the junction temperature. Similarly, the highly loaded converters exhibit an increased junction temperature. Thus the capability to route the power among the different converters is demonstrated.

In the next step, the effect of the power routing on the thermal stress and consequently on the reliability is demonstrated. For this purpose, the reference current  $i_{ref}^*$  is varied for



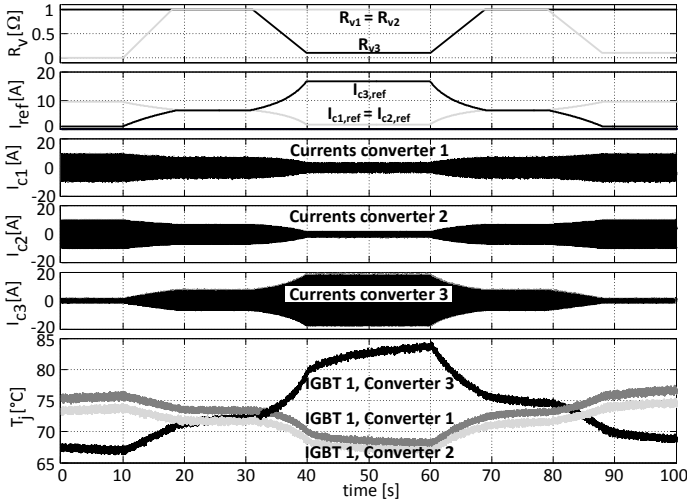


Fig. 15: Measurement: Power routing in three parallel converters by means of virtual resistors for constant output power and a variation of the virtual resistors.

different virtual resistors and the resultant power distribution is shown in (11).

$$\begin{bmatrix} R_{v1} \\ R_{v2} \\ R_{v3} \end{bmatrix} = \begin{bmatrix} 0.5 \\ 0.5 \\ 1 \end{bmatrix} \rightarrow \begin{bmatrix} P_{c1} \\ P_{c2} \\ P_{c3} \end{bmatrix} = \begin{bmatrix} 40 \% \\ 40 \% \\ 20 \% \end{bmatrix} \quad (11)$$

In this case only the current is varied, while all other parameters are kept constant. The power cycle can be seen in the reference value of Fig. 16 as well as in the current distribution among the converters. Again, the measured currents have the same magnitude as the reference current, which demonstrates the functionality of the power routing. The power cycle is causing a thermal cycle in the junction temperature measurements as expected. The thermal cycle shows a proportional behavior to the power distribution, which results in  $\Delta T = 10 K$  for converter 1 and converter 2, while the thermal cycle in converter 3 is only  $\Delta T = 5 K$ . Also the average temperature of converter 3 is reduced.

As a consequence, the lifetime of the power semiconductors is consumed unequally. Following the simple lifetime model expressed in (1), the  $\Delta T$  influences the lifetime consumption exponentially with a factor  $a_2 \approx 5$ , leading to 32 times higher damage for the power semiconductors in converter 1 and 2 in comparison to those in converter 3. This is even amplified with the difference in the average junction temperature, which is also higher for the two highly loaded converters. Consequently, a relatively high remaining lifetime requires only a very small imbalance of the power in the converters. A small remaining lifetime results in the potential to effectively unload the thermal stress from the device for extending its lifetime. Beside the potential, it needs to be pointed out that unequal loading of the devices consumes more lifetime of the system if all damages are summed up.

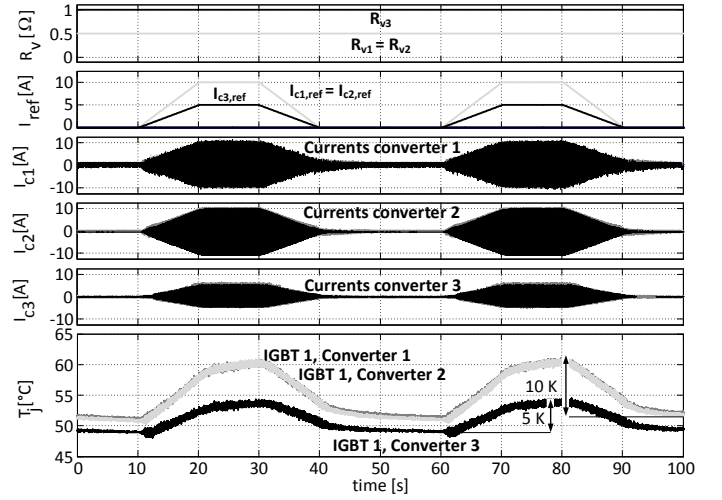


Fig. 16: Measurement: Power routing in three parallel converters by means of virtual resistors for power cycle.

### B. Efficiency impact of power routing

The impact of the power routing on the efficiency of the system is evaluated experimentally in this subsection. For the demonstration of the effects, a Yokogawa WT1800 power analyzer is used to measure the losses of the converter. The losses are measured for the case that two of the converters process the same power, while the power of a single converter is either reduced or increased. The results for the different power distribution and the related losses measurement are shown in Fig. 17 (b), when a single converter is unloaded and when a single converter is overloaded. Due to the open modules, the maximum blocking voltage is limited and thus neither the converter nor the operation point are optimized. For this reason, the losses are normalized on the minimum losses of the converters found during equal power sharing. The power distribution between the converters is visualized in the upper plot and quantified at the x label of the lower plot.

The measurements are obtained for approximately similar junction temperatures of  $T_{j1} = T_{j2} = T_{j3} = 60^\circ C$ . It can be seen that unloading a power converter increases the losses of the converter, which can also be observed for overloading one converter. Nevertheless, the maximum increase in losses is only 0.5 % in the most extreme operating conditions. It needs to be pointed out that this is the worst operation point, while smaller variations in the loading of the converters have a lower increase of the losses. Overloading one converter results in a similar behavior, whereas it needs to be mentioned that not all operation points could be measured because of the high current in the single converter. Nevertheless, the trend, that an increase of the losses results in the reduction of the efficiency is similar to the case of unloading one converter.

## VI. CONCLUSION

This work has proposed the concept of a modular power converter for applications with high reliability demands, such

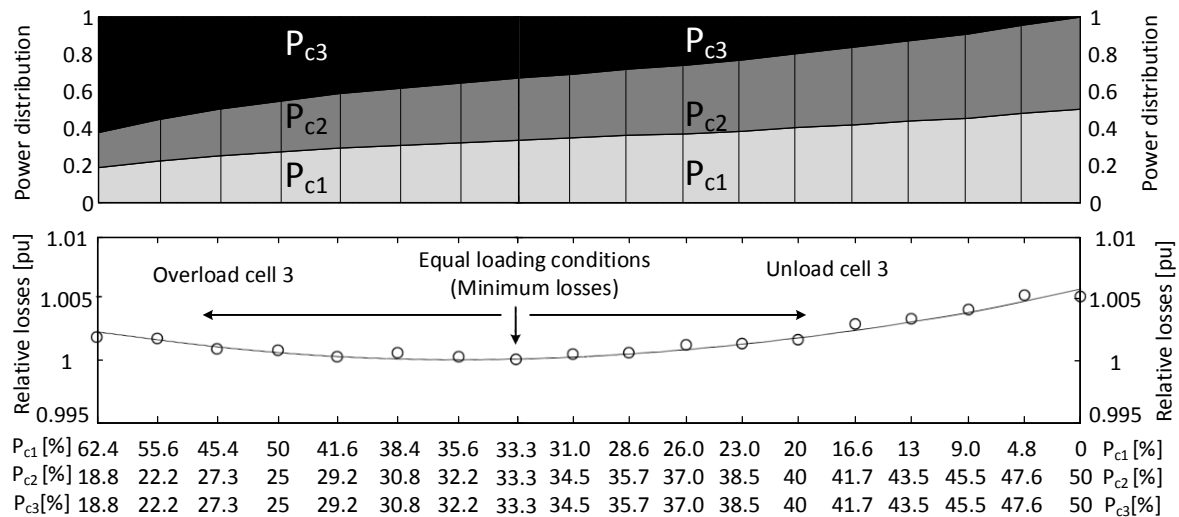


Fig. 17: Measurement: Effect of Power routing on the efficiency of the converter system for unloading one converter and for overloading one converter.

as the ST in the distribution grid. A software based concept for controlling the reliability, the power routing concept, is proposed for controlling the lifetime of the modular building blocks in the ST. By routing the power, the time to the next maintenance can be maximized and the lifetime of the system can be increased by approximately 7.5 – 44% under the investigated conditions. It is experimentally proven that the stress distribution between the parallel parts can be controlled, consequent the wear out of the components. As a price to pay for this increased reliability, the efficiency is slightly reduced for unequally loaded converters. These findings are fully validated with a special set-up, which allows directly accessing the power semiconductor's junction temperature.

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